ARMY TM 11-5895-356-34-1/8

AIR FORCE T.O. 31R2-2TSC38-52-8-1

DIRECT SUPPORT AND GENERAL SUPPORT

MAINTENANCE MANUAL

TRANSMITTER, RADIO T-1021/TSC-38B

(P/O COMMUNICATIONS CENTRAL AN/TSC-38B)

DEPARTMENTS OF THE ARMY AND THE AIR FORCE

MAY 1973

WARNING

HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions.

Learn the areas containing high voltage in each piece of equipment. Be careful not to contact high voltage connections when installing or operating this equipment. Before working inside the equipment, turn power off and ground points of high potential before touching them.

WARNING

DO NOT OPEN THE SEALED VARI-L OVEN IN THE HF VCO ASSEMBLY. IT CONTAINS BERYLLIUM OXIDE, WHICH IS HIGHLY TOXIC IF INHALED.

CAUTION

To prevent permanent damage to the RF translator A1 assembly output transistor, when the transmitter output is not connected to the linear power amplifier, insure that a 50-ohm termination (20-db fixed attenuator) is connected to the transmitter output connector J1.

CAUTION

Support the drawer when separating it from the supporting tracks. Dropping the drawer may cause damage to the equipment.

TECHNICAL MANUAL
No. 11-5895-356-34-1/8
TECHNICAL ORDER
31R2-2TSC38-52-8-1

DEPARTMENTS OF THE ARMY
AND THE AIR FORCE
WASHINGTON, D.C., *30 May 1973*

Direct Support and General Support Maintenance Manual
TRANSMITTER, RADIO T-1021/TSC-38B

		Paragraph	Page
CHAPTER 1.	INTRODUCTION		
Section I.	General	1-1—1-3	1-1
II.	Description and data	1-4	1-2
CHAPTER 2.	FUNCTIONING OF EQUIPMENT		
Section I.	Functional description	2-1, 2-2	2-1
II.	Block diagram analysis	2-3—2-8	2-4
III.	Circuit analysis	2-9—2-15	2-13
CHAPTER 3.	DIRECT SUPPORT MAINTENANCE INSTRUCTIONS		
Section I.	General maintenance information	3-1—3-19	3-1
II.	Troubleshooting at direct support	3-20—3-26	3-7
III.	Maintenance of transmitter	3-27—3-29	3-49
IV.	Direct support testing	3-30—3-32	3-58
CHAPTER 4.	GENERAL SUPPORT MAINTENANCE INSTRUCTIONS		
Section I.	General maintenance information	4-1—4-19	4-1
II.	Troubleshooting at general support	4-20—4-24	4-3
III.	Maintenance of transmitter	4-25—4-28	4-19
IV.	General support testing	4-29	4-33
INDEX			1-1

LIST OF ILLUSTRATIONS

Figure No.	Title	Page
1-1	Radio transmitter T-1021/TSC-38B	1-1
2-1	Passbands for audio channels and 100-kHz pilot carrier	2-2
2-2	Modulator section, block diagram	2-5
2-3	Frequency select section, block diagram	2-9
2-4	Frequency synthesizer (A2), block diagram	2-11
2-5	Channel A1/B1 filter pair A3, schematic diagram	2-14
2-6	Channel A2/B2 filter pair A6, schematic diagram	2-15
2-7	Multiplex carrier generator A9, schematic diagram	2-16
2-8	Preamplifier A1A1, schematic diagram	2-24
2-9	Minus 7-volt voltage regulator A1A6, schematic diagram	2-25
2-10	Filter box A1A4, schematic diagram	2-26
2-11	1-6-MHz VCO variable (÷ N) divider A2A6A1, block diagram	2-41
2-12	Minus 28 Vdc power supply A19, external connections	2-50
3-1	Rack-mounted test setup diagram	3-10
3-2	Transmitter bench test setup diagram	3-19
3-3	Transmitter troubleshooting waveforms guide	3-44
3-4	Transmitter troubleshooting waveforms (4 sheets)	3-45
3-5	Transmitter adjustments	3-50
3-6	Printed circuit card removal with extraction tool	3-56
3-7	Frequency synthesizer A2 removal	3-57
4-1	Synthesizer/test set, connection diagram	4-20
4-2	1-6-MHz control loop adjustment, test equipment setup	4-22
4-3	1-6-MHz control loop waveforms	4-23

Figure No.	Title	Page
4-4	Hf VCO adjustment, test equipment setup	4-25
4-5	Rf section 2nd. L.O. adjustments, test equipment setup	4-26
4-6	Frequency synthesizer A2 cover removal	4-27
4-7	Frequency synthesizer A2, parts location diagram (3 Sheets)	4-28
4-8	Transmitter power supply removal	4-32
FO-1	Color code marking for MIL-STD resistors, capacitors, and inductors	Fold-in
FO-2	Transmitter 6A9/6A11, block diagram	Fold-in
FO-3	Control section, block diagram	Fold-in
FO-4	RF translator A1, block diagram	Fold-in
FO-5	Power supply section, block diagram	Fold-in
FO-6	Dual balanced modulator A7/A21, schematic diagram	Fold-in
FO-7	Control circuits, simplified schematic diagram	Fold-in
FO-8	Signal control A5, schematic diagram	Fold-in
FO-9	Transmit gain control A4, schematic diagram	Fold-in
FO-10	Automatic channel loading A8, schematic diagram	Fold-in
FO-11	Tune leveler circuits, simplified schematic diagram	Fold-in
FO-12	Converter A1A2 (230-20-255) schematic diagram	Fold-in
FO-13	Converter A1A2, (233-20-262) schematic diagram	Fold-in
FO-14	Low-pass filter A1A5, schematic diagram	Fold-in
FO-15	Video amplifier A1A3, schematic diagram	Fold-in
FO-16	Frequency select memory A13, A14, and A15, schematic diagram	Fold-in
FO-17	Band control A16, schematic diagram	Fold-in
FO-18	Code conversion matrix No. 1 (A17), schematic diagram	Fold-in
FO-19	Code conversion matrix No. 2 (A18), schematic diagram	Fold-in
FO-20	Frequency synthesizer A2, detailed block diagram	Fold-in
FO-21	Master clock divider A2A5A1, block diagram	Fold-in
FO-22	Master clock divider A2A5A1, schematic diagram	Fold-in
FO-23	Hf (pump) VCO and 1-6-MHz VCO tuning loops, block diagram	Fold-in
FO-24	Hf VCO A2A3, schematic diagram	Fold-in
FO-25	Control loop A2A3A2 (233-00-274), schematic diagram (sheet 1 of 2)	Fold-in
FO-25	Control loop A2A3A2 (233-00-640), schematic diagram (sheet 2 of 2)	Fold-in
FO-26	Preset A2A3A1, schematic diagram	Fold-in
FO-27	In-lock indicator A2A3A3, schematic diagram	Fold-in
FO-28	5-MHz amplifier A2A1, schematic diagram	Fold-in
FO-29	Harmonic generator and mixer, block diagram	Fold-in
FO-30	Harmonic selector A2A2, schematic diagram	Fold-in
FO-31	Buffer amplifier A2A2A2, schematic diagram	Fold-in
FO-32	Video amplifier and mixer A2A2A3, schematic diagram	Fold-in
FO-33	Logic control A2A2A1, schematic diagram	Fold-in
FO-34	1-6-MHz VCO A2A7, schematic diagram	Fold-in
FO-35	Variable divider synthesizer pump A2A6A1, schematic diagram	Fold-in
FO-36	1-6-MHz phase-lock loop A2A6A2, schematic diagram	Fold-in
FO-37	Second L.O. RF section A2A4 signal generating section, block diagram	Fold-in
FO-38	RF section 2nd L.O. A2A4, schematic diagram	Fold-in
FO-39	Variable divider 2nd L.O. A2A5A2, block diagram	Fold-in
FO-40	Variable divider 2nd L.O. A2A5A2, block diagram	Fold-in
FO-41	RF box No. 1 (A2A5), schematic diagram	Fold-in
FO-42	RF box No. 2 (A2A6), schematic diagram	Fold-in
FO-43	Filter box A2A8, schematic diagram	Fold-in
FO-44	Plus 20 Vdc power supply A11, schematic diagram	Fold-in
FO-45	Plus 6.4 Vdc power supply A10, schematic diagram	Fold-in
FO-46	Transmitter, Radio T-1021/TSC-38B (6A9/6A11), interconnection diagram	Fold-in
FO-47	Frequency synthesizer A2, interconnection diagram (2 sheets)	Fold-in
FO-48	Rf translator A1, interconnection diagram	Fold-in
FO-49	Hf VCO A2A3, interconnection diagram	Fold-in
FO-50	Frequency synthesizer A2, location of test points and adjustments	Fold-in
FO-51	Transmitter chassis assembly (6A9/6A11), parts location diagram (3 sheets)	Fold-in

LIST OF TABLES

Table No.	Title	Page
1-1	Equipment characteristics	1-2
2-1	Frequency control code	2-8
2-2	Variable divider synthesizer pump data	2-10

Table No.	Title	Page
2-3	3-6-MHz oscillator band selection data	2-28
2-4	Organization of frequency synthesizing circuits	2-28
2-5	Control loop frequencies, bands, ranges and divider ratios	2-34
2-6	VDSP timing chart No. 1	2-44
2-7	VDSP timing chart No. 2	2-44
3-1	Cross-reference of circuit block numbers to reference designations	3-3
3-2	Reference designation number locations	3-5
3-3	Special tools for direct support	3-8
3-4	Direct support maintenance test equipment	3-8
3-5	Frequency synthesizer A2 pump frequency checks	3-17
3-6	Frequency synthesizer A2 L.O. frequency digit checks	3-17
3-7	Voltage and frequency measurements	3-36
3-8	Band control card A16 signal inputs	3-42
3-9	Band control card A16 signal outputs	3-42
3-10	Code conversion matrix cards A17 and A18 signal inputs and outputs	3-43
3-11	Adjustment and alignment procedures	3-49
3-12	Printed circuit card adjustments	3-51
3-13	Frequency tuning range, performance standard test	3-60
3-14	Power output, performance standard test	3-61
3-15	Automatic load control (ALC), performance standard test	3-64
3-16	Front panel controls, performance standard test	3-65
3-17	Transmit gain control, performance standard test	3-66
3-18	Power output adjustment, bench performance test	3-70
3-19	Frequency tuning range, bench performance test	3-71
3-20	Automatic load control (ALC), bench performance test	3-72
3-21	Automatic channel loading, bench performance test	3-74
3-22	Transmit gain control, bench performance test	3-74
3-23	Front panel controls, bench performance test	3-75
3-24	Frequency synthesizer, bench performance test	3-76
4-1	Special tools for general support	4-2
4-2	General support maintenance test equipment	4-2

CHAPTER 1

INTRODUCTION

Section I. GENERAL

1-1. Scope

a. This manual covers direct support and general support maintenance of Radio Transmitter T-1021/TSC-38B (assemblies 6A9 and 6A11), hereinafter referred to as either the transmitter or the exciter (fig. 1-1). The term transmitter should not be confused with the associated linear power amplifier. Detailed functions of the equipment are covered in chapter 2. Direct support maintenance, which is accomplished at the operat-

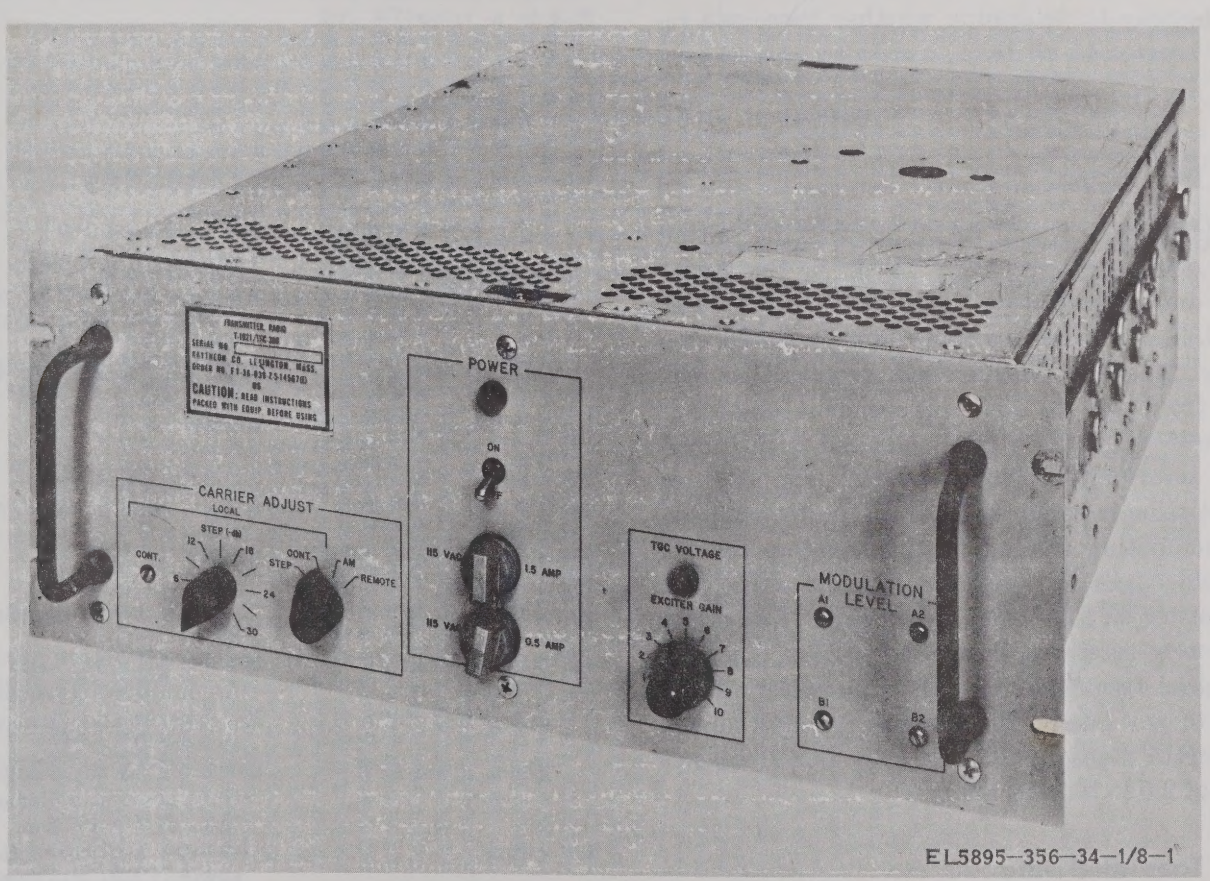


Figure 1-1. Radio Transmitter T-1021/TSC-38B.

ing site, is covered in chapter 3. General support maintenance, primarily accomplished at a fixed maintenance facility, is covered in chapter 4. Tools, test equipment, and materials required are listed for each category of maintenance.

b. Operation and organizational maintenance of this equipment is covered in TM 11-5895-356-12-1 (TO 31R2-2TSC-38-41).

1-2. Indexes of Publications

a. DA Pam 310-4. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.

b. DA Pam 310-7. Refer to DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.

c. TO 0-1-31. USAF personnel refer to TO 0-1-31-series to determine whether there are revisions, changes, additional publications, or Time Compliance Technical Orders (TCTO's) pertaining to the equipment.

NOTE

Applicable forms and records are covered in TM 11-5895-356-12-1.

1-3. Reporting of Equipment Publication Improvements

a. The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submitted on DA Form 2028 (Recommended Changes to Publications) and forwarded direct to Commander US Army Electronics Command, ATTN: AMSEL-MA-CT, Fort Monmouth, N.J. 07703.

b. USAF personnel shall report errors, omissions, and recommendations for the improvement on AFTO Form 22 in accordance with TO 00-5-1.

Section II. DESCRIPTION AND DATA

1-4. Description

Transmitters 6A9 and 6A11 provide the output signal frequency necessary to drive the linear power amplifiers (10-kw PA, unit 2 and 1-kw PA, unit 6A8), respectively. The output signal frequency generated within each transmitter contains from one to four independent sidebands (ISB). Modulation of each sideband with intelligence information (voice or data signals) for transmission is performed within the transmitter. The modulating intelligence information for the four sidebands is supplied separately to each transmitter on four independent lines from either the system receivers or telephone lines. The output signal frequency of each transmitter can be tuned to any one of 280,000 RF channels spaced in discrete steps of 100-Hz over the frequency range of 2.0 to 29.9999 MHz.

1-5. Tabulated Data

Refer to TM 11-5895-356-12-1 for the transmitter operating procedure and a description of the front panel controls and indicators. The equipment characteristics for the transmitter are listed in table 1-1.

Table 1-1. Equipment Characteristics

Parameter	*Characteristics*
Frequency range	2.0000 to 29.9999 MHz
Frequency stability	Internal standard: 1 part in 10^8/day (after 1-hour warmup).
Types of operation	SSB, ISB, compatible AM, CW, FSK.
Number of tunable channels.	280,000
Tuning time	5 seconds (maximum)
Remote tuning control technique.	28-line, digital, 2-out-of-5 code.
Spacing between channels.	100 Hz
Number of audio or data channels.	Four (independently selectable).
Audio frequency response.	350 to 3040 Hz with ± 1.1-db ripple (maximum).
Input impedance	600 ohms, balanced and center-tapped.
Input signal level	Independently adjustable by front panel potentiometer from 0 to +10 dbm.
RF output	0-400-mw peak-envelope-power (PEP) into 50-ohm (nominal) load.
Power requirements	120-Vrms ±10%, 47-420-Hz, single-phase; +27 Vdc at 0.5A.
Automatic load control (ALC).	Reduces transmitter gain to minimize output power excursions resulting from

Parameter	*Characteristics*
	input signals with high peak-to-average ratios. A control voltage from the external rf power amplifier in the range 0 to −10 volts (corresponding respectively to a −0.5 and +0.5 db variation in the nominal PEP) reduces the gain by 0 db to a minimum of 20 db. ALC function can be disabled by ALC switch.
Transmitter gain control (TGC).	Controls the transmitter output power to insure that the overall power output of the linear power amplifier associated with the transmitter is held constant between 2 and 29.9999 MHz. This control is provided by a dc voltage applied from the linear power amplifier to the transmitter. Whenever a change in output occurs, TGC corrects the change within 200 ms. TGC can be preset to control the transmitter output signal level between 40 and 400 mw. A toggle switch located on the transmit gain control card within the transmitter can disable TGC when it is not required.
Automatic channel loading (ACL).	Automatically changes transmitter gain for any combination of audio channels selected to maintain correct overall peak envelope power (PEP) and allowing only minimum variations above maximum peak envelope voltage (within ALC threshold region).
Carrier suppression (pilot carrier disabled).	55 db (minimum) below rms power of single tone at full-rated output.
Pilot carrier suppression: Selected with front panel	Adjustable in steps of 3 ±2 db from 0 to −30 db.
CARRIER ADJUST-LOCAL switch in the STEP position and the STEP (−db) switch set to a selected value.	
Adjusted by front panel CONT. potentiometer with CARRIER ADJUST-LOCAL switch set to CONT.	
Adjusted in steps at secondary mode and status panel (7A5/7A12) by XMTR PLT CARR switch with CARRIER ADJUST-LOCAL switch set to REMOTE.	−30 db, −20 db, 0 db and VAR.
Undesired signal suppression:	
Adjacent channel interference.	Unwanted sidebands and adjacent channel energy suppressed −45 db (minimum); −35 db referenced to nominal PEP.
Harmonics	−40 db below nominal PEP
Spurious emissions noise.	At the RF output, the total average noise in a 3-kHz bandwidth is 50 db below average power of signal tone which produces full-rated output.
Intermodulation distortion.	Third and higher order distortion suppressed 40 db (minimum) below either of two tones.
Envelope delay distortion (+15° to +55° C, each channel).	1 ms, 600–2700 Hz; 4 ms, 350–3040 Hz.
RFI	Meets the requirements of MIL-I-11748B.
Physical characteristics:	
Size	7″ high x 19″ wide x 22″ deep.
Weight	65 lbs (approx.)
Mounting	19″ relay rack
Operating environment:	
Temperature range	0° to +55° C
Vibration	MIL-T-4807, method A
Fungus	Nonnutrient
Humidity	MIL-E-5272, Proc. II to 10,000 ft.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. FUNCTIONAL DESCRIPTION

2–1. General

This chapter provides general and detailed functional descriptions for the transmitter. The transmitter accepts audio and/or data input signals and produces a modulated signal in the frequency range of 2.0–29.9999 MHz. The modulated signal is applied to an external RF power amplifier which raises the amplitude of the signal to a level suitable for transmission. The external stage functions as a linear power amplifier (LPA), and does not introduce changes in the frequency. Except for some calibration or setup controls which are mounted on the front panel of the transmitter, the controls normally used in conjunction with the transmitter unit are physically located on a separate control panel. The general functional analysis describes the overall transmitter functioning, and is supported by a functional block diagram. Following the general functional analysis is a detailed functional analysis, which describes the various circuits comprising the transmitter.

2–2. Transmitter 6A9/6A11 (fig. FO–2)

The transmitter is divided into six main sections (fig. FO–2): modulator, control RF translator (A1), frequency select, frequency synthesizer (A2), and power supply.

a. Modulator. The modulator uses the 4-channel audio signals to modulate three carriers. One carrier is a 100-kHz signal supplied to the modulator from the frequency synthesizer. This 100-kHz signal serves as the carrier for the two inboard channels (A1 and B1). The other two carriers are generated within the modulator, and serve as carriers for the outboard channels (A2 and B2), and appear at 106.290 and 93.710 MHz respectively. As shown in figure 2–1, all four channels are nominally 3.0 kHz wide, and are symetrically arranged around the 100-kHz carrier. Each channel may be enabled separately, and the modulation level for each channel may be adjusted independently. This is accomplished through the use of the channel enable signals and the modulation level adjust signals which are applied to the modulator circuits. The modulator produces up to four independent sideband (ISB) signals containing the input audio information. These ISB signals are then supplied to the control section.

b. Control. The Control section controls the level of the combined ISB signals and the level of the carrier used in the RF translator during tuneup and transmitting modes. The control section also permits selection of operating modes and modulation types with either local or remote control options. The control section receives inputs from the linear power amplifier, the transmitter front panel, the mode and status panel 7A5/7A12, the frequency synthesizer (A2), the modulator, and the RF translator (A1).

(1) Input signals to the control are as follows:

(*a*) *Transmitter key.* The transmitter key signal enables the control section, allowing the signal to be coupled to the RF translator.

(*b*) *ALC sample.* The ALC sample signal is a dc sample of detected transmitter modulation envelope; part of the automatic load control circuit used to prevent overdriving of the LPA.

(*c*) *TGC sample.* The TGC sample signal is a dc sample of detected modulation envelope; part of transmit gain control circuit used to maintain overall gain of transmitter/LPA at constant level.

(*d*) *Carrier adjust.* The carrier adjust signal adjusts level of carrier insertion. In remote mode, adjustment is supplied to control section from the mode and status panel (7A5/7A12); otherwise, adjustment is from the transmitter front panel.

(*e*) *Transmitter gain control.* Manual control used to set the reference for the range of control of the TGC circuit.

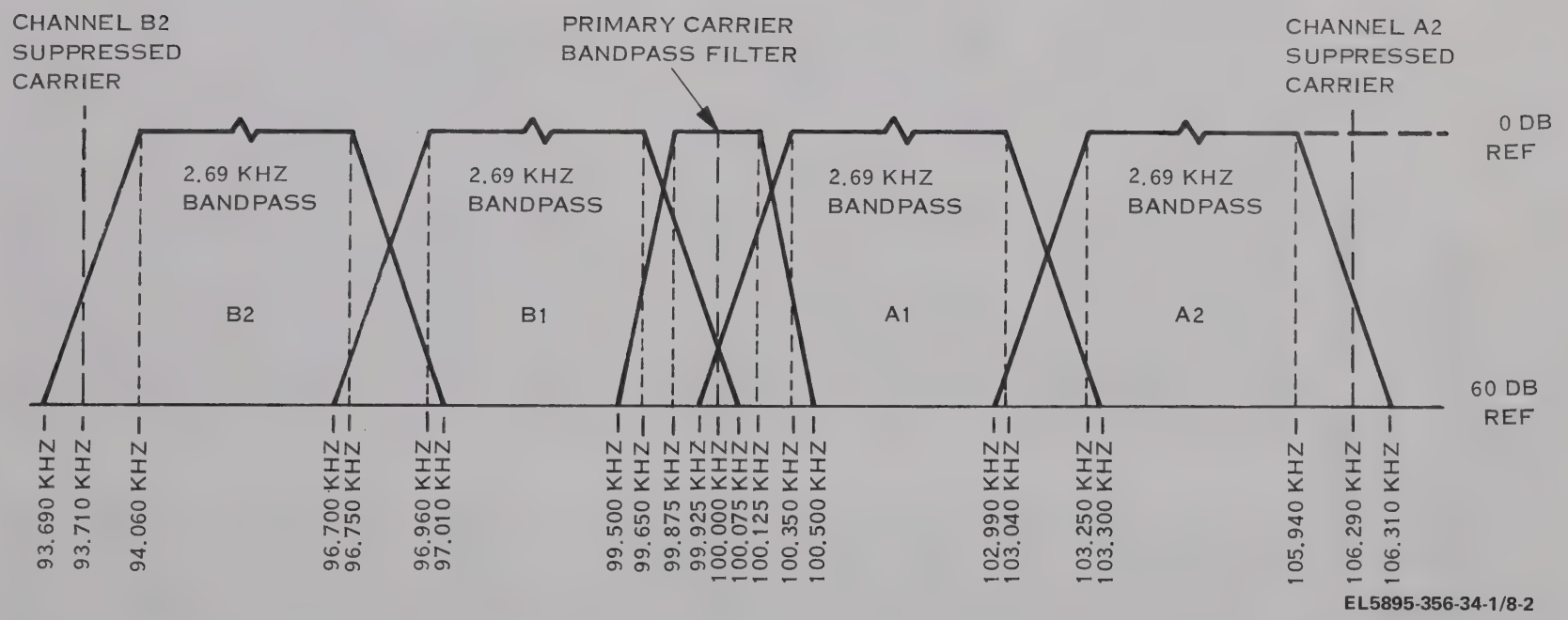


Figure 2–1. Passbands for audio channels and 100-kHz pilot carrier.

(*f*) *Channel enable.* Enabling signals from the mode and status panel (7A5/7A12) for channels A1, B1, A2, and B2.

(*g*) *Carrier enable.* Enables carrier amplifier circuitry to permit insertion of carrier component into signal train.

(*h*) *Tune enable.* Control signal from LPA; permits carrier-only signal to be routed at a fixed level through the transmitter to the LPA while the LPA is in the tuning mode.

(*i*) *ISB signals (4).* Audio input signals from the mode and status panel (7A5/7A11) for modulating channels A1, B1, A2, and B2.

(*j*) *100-kHz carrier.* Carrier signal from the frequency synthesizer (A2).

(*k*) *Tune leveler.* Sample voltages from the RF translator (A1) for the tune leveler loop. This loop is used during transmitter tuning to provide a control voltage which maintains the carrier amplitude at a constant preset level.

(2) Output signals from the control section include—

(*a*) TGC and AGC signals going to the RF translator (A1).

(*b*) Output RF level control signal going to the mode and status panel (7A5/7A12).

(*c*) Reset signal to the frequency select section.

(*d*) ISB and/or carrier signals to the RF translator (A1).

(3) The transmitter is normally operated in the suppressed carrier mode (carrier enable off). It can also be adjusted to permit a portion of the carrier to be transmitted, or can provide compatible am operation. Compatible am is defined as transmission of a single-upper sideband of intelligence with the carrier voltage suppressed 6 db below the peak RF power.

(4) Control of the RF output is accomplished manually by the EXCITER GAIN control on the transmitter front panel (fig. 1–1), and automatically by a form of AGC which is based on the level of the audio modulation being transmitted. The EXCITER GAIN control is used primarily for establishing a control range rather than as an operating control. For automatic control, the modulation is sampled by means of the ALC (automatic load control) signal. This is a detected voltage which represents that portion of the transmitter modulation envelope level which exceeds the rated output of the transmitter. The voltage is derived from signals processed in the LPA, which is external to the transmitter. The ALC signal then controls the level of the sideband energy supplied to the RF translator (A1) to insure that the LPA is not overdriven on peaks of the input signal.

(5) The channel enable signals also set the gain of the control section input stage to reduce the multiplexed input signal level as more channels are enabled. This operation is called automatic channel loading (ACL). As each channel is enabled, the increase in input signal level is compensated for by the reduced gain. Hence, the transmitter average output level is held nearly constant and the ALC dynamic range is preserved for control of modulation excursions.

(6) The TGC (transmit gain control) input signal, also a detected voltage, is dependent upon the instantaneous level of the envelope power being transmitted. This signal, which is similarly derived from the LPA, is fed back to the control section and compared with the instantaneous level of the composite signal consisting of the sideband and any carrier energy present. The resulting error (or AGC) signal is then routed to the RF translator (A1), where it is used to insure that the overall transmitter gain remains contant regardless of frequency or environmental conditions.

(7) The dc tune leveler signal from the RF translator (A1) is processed within the control section to provide a control voltage for the tune leveler loop, and an output signal for a level indicator on the mode and status panel (7A5/7A12).

c. RF Translator. The ISB and/or carrier signal output of the control section is applied to the RF translator (A1) where it is translated in a two-step operation to the transmitted frequency. The L.O. and pump signal outputs of the frequency synthesizer (A2) are used in this process. The 90.8990–90.8999 MHz L.O. signal is mixed with the nominal 100-kHz signals to provide the nominal 91-MHz IF signal. The 61–88.999 MHz pump signal is mixed with the 91-MHz IF signal to provide the output frequency in the 2.0–29.9999-MHz hf range. The RF translator (A1) output signal level is sufficient to drive the external LPA, which in turn raises the signal level to an amplitude suitable for transmission. The RF translator (A1) also provides a rectified voltage to the control section for use in the tune leveler loop and as a signal indicating output level for display on the mode and status panel (7A5/7A12). The AGC input from the control section is a composite of the TGC error voltage

and the reference voltage from the EXCITER GAIN control potentiometer on the transmitter front panel.

d. Frequency Select Section. The frequency select section stores the digital frequency selection signals supplied from the frequency select panel (7A4/7A11) and decodes the stored information to provide frequency control signals to the frequency synthesizer (A2). The Xmtr tune signal which is applied manually from the frequency select panel (7A4/7A11) initiates the transmitter tuning cycle by resetting the selection circuitry of the frequency select section.

e. Frequency Synthesizer (A2). The frequency synthesizer (A2) accepts the decoded control signals from the frequency select section to tune the L.O. and pump signals to the correct frequencies required by the Rf translator (A1). It also provides a 100-kHz signal for reference in the modulator and for use as the center carrier in the control section. The digital tune enable signal from the Frequency Select section is applied to the frequency synthesizer (A2) to initiate a predetermined scanning sequence required to lock onto the selected frequency. During the tuning process, the frequency synthesizer (A2) generates a digital tune-in-progress (DTIP) signal for display on the mode and status panel (7A5/7A12). The DTIP signal is routed via the power supply section.

f. Power Supply. The power supply section contains three power supplies which operate on 120 Vac, 47–420 Hz to provide +20, +6.4, and −28 VDC power required in the transmitter circuits. The DTIP line is interlocked in the power supply to prevent false indications when transmitter power is off.

Section II. BLOCK DIAGRAM ANALYSIS

2–3. Modulator
(fig. 2–2)

The modulator modulates the reference carriers with the audio intelligence from those channels of the four inputs which have been enabled. The modulator then generates the appropriate independent sidebands. The audio inputs are converted from frequencies in the range of 350–3040 Hz to frequencies in the ranges of 100.35 to 103.04 kHz (channel A1), 99.65 to 96.96 kHz (channel B1), 105.94 to 103.25 kHz (channel A2), and 96.75 to 94.06 kHz (channel B2). The four audio channels are enabled by ground-online inputs from the four channel enable switches on the mode and status panel (7A5/7A12). Audio inputs for channels A1 and B1 are applied through separate front panel gain controls to the channel A1 and B1 dual balanced modulators (A7). The modulators are separate circuits that are packaged in pairs to provide translation and modulation for both channels. In the channel A1–B1 modulators (A7), the audio signals are mixed with the 100-kHz injection frequency from the frequency synthesizer (A2) and then filtered to yield the ISB suppressed carrier outputs. Audio inputs for channels A2 and B2 are processed similarly in dual balanced modulator (A21), except that the reference carrier inputs of 106.29 kHz (A2) and 93.71 kHz (B2) (the outboard upper and lower sidebands respectively) are supplied by the multiplex carrier generator (A9) module. Both filter pairs (A3 and A6) are dual units that provide the correct selectivity and channel shaping characteristics for the four sideband signals. The filtered outputs, in the frequency ranges noted above and with the carrier frequencies stripped off, are routed to the control section.

2–4. Controls
(fig. FO–3)

The control section incorporates automatic and manual switching circuits, portions of gain control loops, and amplifiers for the sideband and carrier signals. The switching circuits permit selection of operating modes and modulation types with both local and remote control options. The gain control loops maintain the desired transmitter gain and peak-power output. Other circuits provide automatic channel loading for the four channels, maintain a desired signal level at the transmitter output for tuning purposes, and enable manual control of the transmitter output level. As shown in figure FO–3, the control section accepts the following signal inputs:

a. ISB signals from the four bandpass filters in the modulator.

b. 100-kHz carrier signal from the frequency synthesizer (A2).

c. Tune enable signal from the LPA for the duration of the LPA tuning cycle.

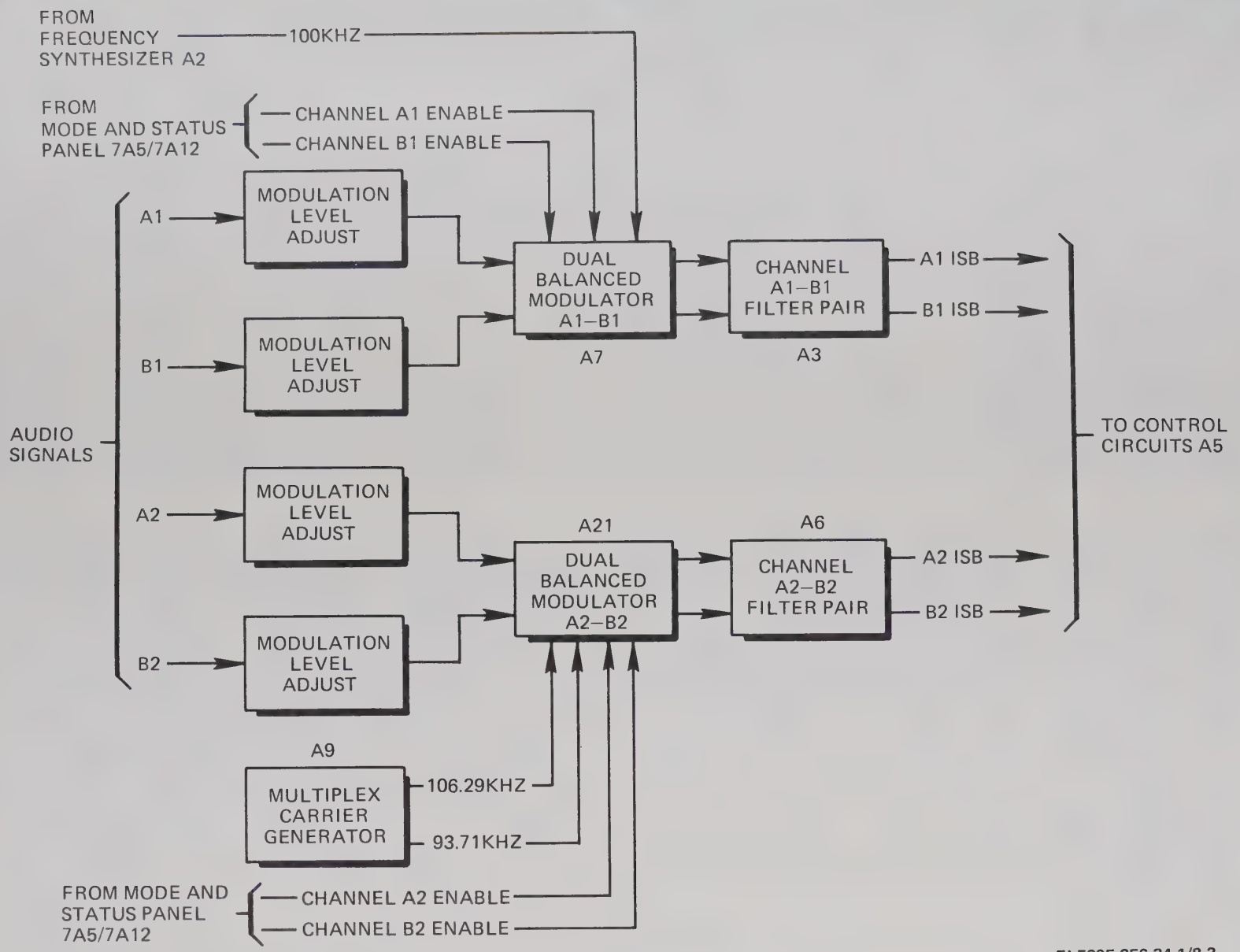


Figure 2–2. Modulator section, block diagram.

d. ALC (automatic load control) sample voltages from the LPA portion of the ALC gain control loop.

e. TGC (transmit gain control) sample voltages from the LPA portion of the TGC loop.

f. Sample voltages from the RF translator (A1) detector for the tune leveler loop.

g. Manually applied control or calibrating inputs from the mode and status panel (7A5/7A12).

(1) The control section outputs include a signal which is applied to the RF translator (A1) and may be in the form of an ISB signal with partially or fully-suppressed carrier, a high-level carrier with an upper sideband (compatible AM), or a carrier-only signal with no sidebands. Other outputs are the TGC signal supplied through the AGC amplifier to control the RF translator gain, and a dc signal proportional to the RF level, which is supplied from the tune leveler input circuit to the mode status panel (7A5/7A12) NORMAL LEVELS meter.

(2) The ISB signals and the 100-kHz carrier undergo controlled gain amplification from the input through the signal amplifier output. The ISB signals from the modulator are applied to the input section through the multiplex combiner. This circuit sums the four ISB signals into a composite signal. The combined signal is then scaled by the ACL circuit, amplified by the ALC'd amplifier, and routed through modulation disable relay K1 to the signal amplifier. The 100-kHz carrier is applied to the signal amplifier via the carrier amplifier. When the carrier enable signal is applied from the mode and status panel (7A5/7A12), the 100-kHz signal is passed to the signal amplifier for amplification and impedance matching, and then to the RF translator (A1). The carrier amplifier gain is controlled to set the level of the carrier in the transmitter output.

(3) The ACL stage, in series with the multiplex combiner, automatically provides a nearly constant input signal level to the ALC'd amplifier regardless of the number of channels selected. The amplitude of the composite signal at the output of the multiplex combiner depends upon the number of ISB channels enabled, since the signal levels of each channel usually are set equal. To compensate for changes under all input conditions, the combined signals are routed through the ACL amplifier, whose gain is varied in relation to the number of channels enabled.

(4) The ALC loop circuits ensure that the modulation envelope level does not exceed transmitter rated output by more than 0.5 db, regardless of peaks in audio signal input level. The ALC loop circuits in the control section include the dc inverter, ALC ENABLE switch S1, and ALC'd amplifier. The ALC sample voltage is a rectified RF signal which represents that portion of the transmitter modulation envelope level that exceeds rated output. This voltage is supplied via the dc inverter to control the bias on one of the stages of the ALC'd amplifier. Switch S1 is used to disable the ALC loop for calibration purposes.

(5) The TGC loop circuits maintain overall gain of the transmitter/LPA at a constant level. The TGC loop circuits in the control section include the TGC reference amplifier, differential amplifier, TGC memory, and digital-to-analog (D–A) converter (fig. FO–3). The TGC circuits sample and compare the level of incoming modulation and the level of LPA modulation output. The TGC reference amplifier accepts the modulation signal from the signal amplifier, scales and detects the modulation envelope, and supplies the resultant signal to the differential amplifier. The differential amplifier also receives the TGC sample voltage derived from the LPA output, and compares the two levels to determine the gain of the transmitter. If the gain is not equal to a value predetermined by the loop constants, the comparison yields a loop-error signal. This signal acts to vary the transmitter gain to return the overall gain to the predetermined value. To accomplish this the error signal controls the status of the TGC memory, a five-stage counter. The memory provides long-term storage of the digital quantity, which represents the present gain of the transmitter. The digital quantity is converted to an analog voltage in the D–A converter and applied as a control bias to one of the stages in the signal amplifier, and to a 91-MHz amplifier in the RF translator (A1). By varying the gain in this manner, the TGC loop compensates for long-term gain variations, and also gain variations across the tuning range, thus assuring a constant transmitter output power level with fixed audio drive level.

(6) Other inputs manually applied from the mode and status panel (7A5/7A12) include: the channel enable, transmitter key, and carrier enable, which are ground-on-line signals, and the carrier adjust, which is a variable voltage level. The transmitter chassis manual controls

shown in figure FO–3 include CARRIER ADJUST STEP (−db) switch S302, CARRIER ADJUST select switch S303, CARRIER ADJUST CONT potentiometer R305, and EXCITER GAIN potentiometer R318. Tune control relay K302 provides interlocking and automatic routing functions for the tune enable and various other signals, as discussed in the following paragraphs.

(7) The tune enable signal (supplied automatically from the LPA) energizes modulation disable relay A5K1, tune control relay K302, and tune level relay A8K1. Energizing A5K1 removes all ISB inputs to the signal amplifier. Energizing K302 provides a transmitter key signal which enables the signal amplifier output stage, enables the carrier, and also causes the TGC memory circuit to be reset to a value close to its minimum gain point. This permits routing of only the 100-kHz carrier signal from the carrier amplifier through the signal amplifier. Energizing of A8K1 by the tune enable signal from the LPA provides continuity for a constant level signal that controls the gain of the RF translator (A1). It also closes an AGC feedback loop that maintains a fixed transmitter output level by controlling the gain of an amplifier in the signal control module A5. When the transmitter is not in the tune enable mode, A8K1 is deenergized and the signal amplifier is again controlled by the TGC loop.

(8) The transmitter key signal directly enables the output stage of the signal amplifier, which couples any signal appearing at that point to the RF translator (A1). The keying function is also provided through relay K302 whenever the tune enable signal is applied.

(9) The carrier enable signal energizes the carrier amplifier to permit insertion of a 100-kHz carrier signal at a desired level into the signal amplifier circuit. Whenever the tune enable signal is applied, the carrier enable function is provided simultaneously through contacts on relay K302.

(10) The carrier adjust signal is a variable dc voltage which controls the level of carrier insertion. The voltage is applied as a control signal to the carrier amplifier.

(11) The automatic gain control circuit between the D–A converter and the signal amplifier is concerned primarily with the overall gain in the RF translator (A1). When the transmitter is in operation, the gain of the RF translator (A1) is controlled by the TGC loop and EXCITER GAIN potentiometer R318 on the transmitter front panel. During the tune enable mode (when the TGC is disabled) a dc level from a voltage divider provides fixed bias to a buffer stage, enabling the buffer output to override the level set by potentiometer R318. Control is accomplished by tune level relay A8K1, which is energized by the tune enable signal. The relay contacts provide a path for AGC feedback of the detected transmitter output level to the signal amplifier on the signal control module A5. This feedback maintains transmitter output at a constant level. The tune leveler dc amplifier, A8Q1, also provides an output signal for the NORMAL LEVELS meter on the mode and status panel (7A5/7A12).

2–5. RF Translator
(fig. FO–4)

The RF translator (A1) contains the signal processing elements shown in figure FO–4. The nominal 100-kHz ISB signal from the control section is mixed with the L.O. signal from the frequency synthesizer (A2) to produce the nominal 91 MHz intermediate frequency. The L.O. signal, routed through a buffer amplifier, is a stable frequency ranging from 90.8990 to 90.8999 MHz in 100-Hz steps. To insure rejection of L.O. frequency components in the IF signal, a crystal filter in the mixer output attenuates signals of 90.8999 MHz ±1 kHz. The 91-MHz signal is passed through a 20-kHz bandpass filter for bandwidth definition and reduction of undesired mixer products. The IF signal is then amplified in a 91-MHz IF amplifier. This is an AGC'd stage with variable gain characteristics. The output from this stage is applied to the balanced (second) mixer. The second input to the mixer is the pump signal obtained from the frequency synthesizer (A2) via the pump buffer amplifier. This signal ranges from 88.999 to 61.000 MHz. The output of the balanced mixer is the desired hf signal for transmission, corresponding to the frequency selection set in by the digital control inputs from the frequency select panel (7A4/7A11). The hf signal is then routed through a low-pass filter for attenuation of frequencies above 30 MHz, and is then applied to the preamplifier. This stage provides approximately 10 db of gain with a flat response over the range of 2–30 MHz. The next stage, the video amplifier, raises the RF signal level to 400-mw PEP in six stages, for routing to the LPA. The RF output is also routed through a detector and to the control section for application to the tune leveler circuit, and further routing

to the NORMAL LEVELS meter on the mode and status panel (7A5/7A12). Circuit elements of the RF translator (A1) are mounted on six assemblies: a converter A1A2 module containing the first mixer, crystal filter, bandpass filter, balanced mixer, L.O. buffer amplifier, and pump buffer amplifier; a broadband preamplifier A1A1 module; video amplifier A1A3 module (containing six amplifier stages and a detector); a voltage regulator A1A6 module which furnishes −7 Vdc to the video amplifier A1A3; a low-pass filter A1A5; and a filter box A1A4 assembly providing routing and filtering elements for the −28 Vdc power circuitry and other inputs and outputs.

2–6. Frequency Select Section (fig. 2–3)

The frequency select section stores the digital frequency selection signals from the frequency select panel (7A4/7A11), and converts the stored information into control signals for tuning the frequency synthesizer (A2). The frequency select section consists of three frequency select memories A13, A14, and A15, a band control A16, two code conversion matrices A17 and A18, and a reset generator which is located on the TGC module (A4).

a. The frequency select memories (A13, A14, and A15) are three identical printed circuit (PC) cards. One accepts signals that represent the digit selected in the 10-MHz place, and signals representing the digit selected for the 1-MHz place. The digit information for the 100-kHz and 10-kHz places is supplied to the second frequency select memory card on five lines for each set. Five lines each are also supplied to the third frequency select memory card for the 1-kHz and 0.1-kHz (100-Hz) places. The digital signals are supplied in a two-out-of-five code which requires that two, and only two, lines be energized out of the five lines representing a given digit. The various patterns and the digits they represent are listed in table 2–1. The 10-MHz digit, which has only three lines, is a special case of the two-out-of-five code. The pattern for the 10-MHz digit is also listed in table 2–1.

b. The digital frequency selection signals may be supplied continuously, but have no effect until the digital tune enable (DTE) signal is applied. Thus, even though the pattern of signals is varied at the frequency select panel (7A4/7A-11), the transmitter does not retune unless the DTE signal is also present. The DTE signal triggers the reset generator, which resets all circuits of the frequency select memories and allows the frequency information from the frequency select panel to be read in. The reset generator is located physically on the transmit gain control (A4) PC card in the control section, but is not associated with it electrically.

c. The output of frequency select memory No. 1 (A13) is decoded in the band control (A16) to produce band and frequency control signals for the frequency synthesizer (A2). The band control (A16) uses the tens-of-MHz and units-of-MHz information to produce the following control signals for routing to the frequency synthesizer (A2).

(1) HF (*pump*) *VCO band* (*preset*) *signals* (*six logic lines*). These select one of six preset frequency bands within the 88.999–61 MHz range of the HF (pump) VCO. Each band is energized by an individual preset circuit.

NOTE

The frequency synthesizer (A2) incorporates several voltage-controlled oscillators (VCOs) which operate at various frequencies. The signal supplied by the HF (pump) VCO is not in 2–30-MHz range but in the 88.999–61-MHz range. It is designated as the HF (pump) signal to differentiate it from the outputs of the other VCO's, which operate at lower frequencies.

Table 2–1. Frequency Control Code

10-MHz digit selected	Control line A	B	C
0	0	x	x
1	x	x	0
2	x	0	x

1-MHz, 100-kHz, 10-kHz, 1-kHz, or 0.1-kHz, digit selected	Control line A	B	C	D	E
0	0	x	0	0	x
1	x	x	0	0	0
2	x	0	x	0	0
3	0	x	x	0	0
4	0	x	0	x	0
5	0	0	x	x	0
6	0	0	x	0	x
7	0	0	0	x	x
8	x	0	0	x	0
9	x	0	0	0	x

NOTE

x indicates a ground on control line; 0 indicates open circuit.

(2) *Mixer injection signals.* These are the same signals as those applied to the preset circuits, and are used to select the appropriate har-

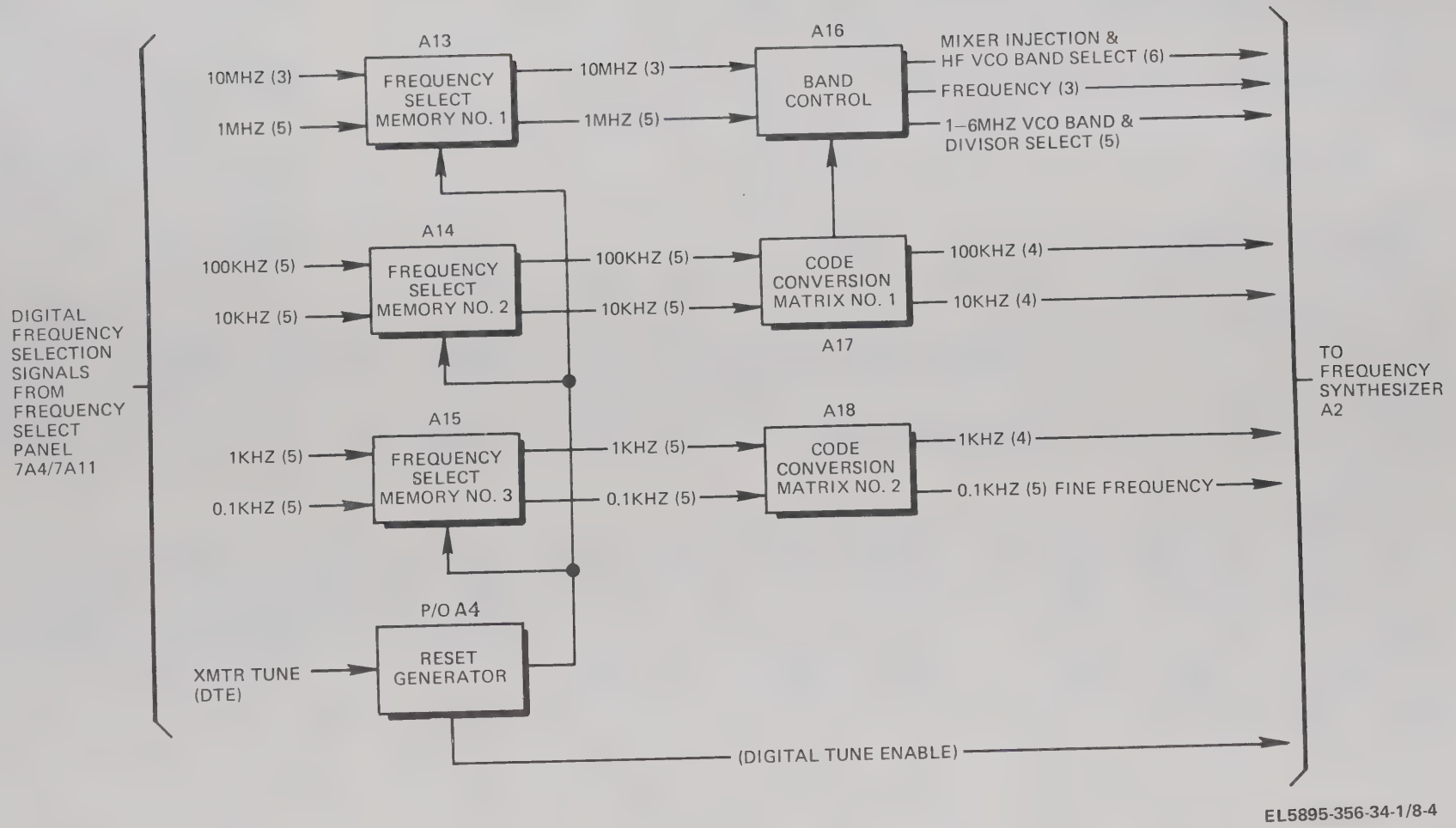


Figure 2–3. Frequency select section, block diagram.

monic frequency (90, 85, 80, 75, 70, or 65 MHz) developed by the harmonic generator.

(3) *1–6-MHz VCO band selection signals.* These determine in which of three bands the 1–6-MHz VCO circuit should operate. The selection is made by means of voltages on two logic lines.

(4) *1–6-MHz VCO divisor selection signals.* These determine which of three divisors (÷1, ÷2, or ÷4) is to be used to obtain the desired frequency output of the 1–6 MHz VCO circuit. The selection is made on three logic lines.

(5) *Frequency selection signals for the variable divider synthesizer pump (VDSP).* The signals, applied on three logic lines, select the first digit of the VDSP division ratio (1, 2, 3, 4, 5, or 6).

d. The units-of-MHz signal from frequency select memory number 1 (A13), and a processed hundreds-of-kHz signal from code conversion matrix No. 1 (A17) are decoded to produce frequency control signals which help to select the proper division ratio in the 1–6-MHz VCO phase-locked loop circuit, and the proper operating range of the 1–6-MHz VCO. The VCO operates in three bands over the range of 3 to 6 MHz. Its output frequency, depending upon the inductor or combination of inductors selected, is 3 to 3.8 MHz (Band A), 3.8 to 4.8 MHz (Band B), or 4.8 to 6 MHz (Band C). The final frequency is within the range of 1 to 6 MHz and is determined by the appropriate combination of band and division ratio (see table 2–2). The ÷K divider can provide three outputs, as follows: ÷4, ÷2, ÷1. Selection of the desired frequency band and divider is accomplished by signals routed on five lines to the 1–6-MHz VCO section.

e. The code conversion matrices (A17 and A18) are contained on two PC cards. One decodes the 100-kHz and 10-kHz outputs from frequency select memory No. 2 (A14); the other decodes the 1-kHz and 0.1-kHz (100-Hz) outputs of frequency select memory No. 3 (A15). The 100-, 10-, and 1-kHz outputs of the code conversion matrices are supplied to the frequency synthesizer (A2) to control the variable divider in the 1–6-MHz VCO phase-lock loop. The 100-kHz output is also routed to the band control (A16) PC card to select the desired band in the 1–6-MHz VCO. The 100-Hz output controls a variable divider in the 90.899-MHz L.O. signal generator.

Table 2–2. Variable Divider Synthesizer Pump Data

Freq. setting (MHz)	Division ratio	Required preset	Equivalent binary word for preset			
2.000	1001	4999	100	1001	1001	1001
2.001	1002	4998	100	1001	1001	1000
2.002	1003	4997	100	1001	1001	0111
2.003	1004	4996	100	1001	1001	0110
2.004	1005	4995	100	1001	1001	0101
2.005	1006	4994	100	1001	1001	0100
2.006	1007	4993	100	1001	1001	0011
2.007	1008	4992	100	1001	1001	0010
2.008	1009	4991	100	1001	1001	0001
2.009	1010	4990	100	1001	1001	0000
2.010	1011	4989	100	1001	1000	1001
2.011	1012	4988	100	1001	1000	1000
↕	↕	↕	↕	↕	↕	↕
2.090	1091	4909	100	1001	0000	1001
2.100	1101	4899	100	1000	1001	1001
2.999	2000	4000	100	0000	0000	0000
3.000	2001	3999	011	1001	1001	1001
3.999	3000	3000	011	0000	0000	0000
4.000	3001	2999	010	1001	1001	1001
4.999	4000	2000	010	0000	0000	0000
5.000	4001	1999	001	1001	1001	1001
5.999	5000	1000	001	0000	0000	0000
6.000	5001	0999	000	1001	1001	1001
6.999	6000	0000	000	0000	0000	0000
7.000	1001	4999	100	1001	1001	1001
7.999	2000	4000	100	0000	0000	0000
8.000	2001	3999	011	1001	1001	1001
8.999	3000	3000	011	0000	0000	0000
9.000	3001	2999	010	1001	1001	1001
9.999	4000	2000	010	0000	0000	0000
10.000	4001	1999	001	1001	1001	1001
10.999	5000	1000	001	0000	0000	0000
11.000	5001	0999	000	1001	1001	1001
11.999	6000	0000	000	0000	0000	0000
12.000	1001	4999	100	1001	1001	1001
16.999	6000	0000	000	0000	0000	0000
17.000	1001	4999	100	1001	1001	1001
21.999	6000	0000	000	0000	0000	0000
22.000	1001	4999	100	1001	1001	1001
26.999	6000	0000	000	0000	0000	0000
27.000	1001	4999	100	1001	1001	1001
29.999	4000	2000	010	0000	0000	0000

2–7. Frequency Synthesizer A2 (fig. 2–4)

The frequency synthesizer (A2) consists of three functional sections: an L.O. signal generating section; and a master clock signal generating section. Inputs for the frequency synthesizer (A2) are supplied as tuning control signals from the frequency select section. All of the circuits comprising the frequency synthesizer (A2) are contained in a single assembly. The frequency synthesizer (A2) also generates a system tuning (DTIP) signal which is applied to the mode and status panel (7A5/7A12) after passing through the power supply section.

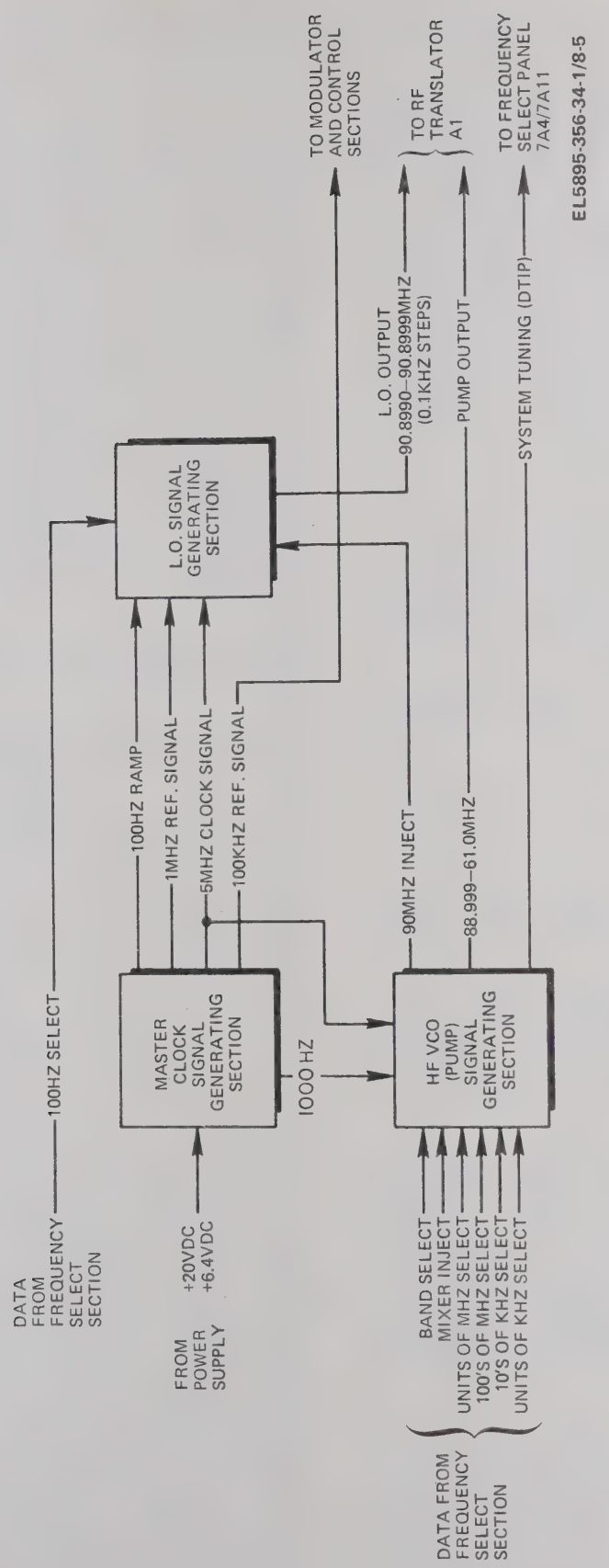


Figure 2-4. Frequency synthesizer (A2), block diagram.

a. Synthesizer Outputs. The frequencies generated within the frequency synthesizer for use outside of the synthesizer are—

(1) A stable L.O. output signal in the range of 90.8990 to 90.8999 MHz. This signal is stepped in 100-Hz steps, and goes to the RF translator (A1) section.

(2) A stable pump output signal to the RF translator (A1). This frequency is in the range of 61.000 to 88.999 MHz and is stepped in increments of 1000 Hz.

(3) A stable 100-kHz reference signal to the modulator section (A7) to supply the carrier for the A1/B1 channels during the modulation process.

(4) A stable 100-kHz signal to the control circuits for use in the partially suppressed mode or in the full carrier (compatible AM) mode.

b. Internal Synthesizer Signals. The frequency synthesizer (A2) also generates the following frequencies for use as references within the function:

(1) A stable 1-MHz signal to the L.O. signal generating section for use as the basic L.O. signal reference.

(2) A 100-Hz ramp reference signal to the signal generating section for L.O. frequency control.

(3) A 1000-Hz reference signal to the HF VCO (pump) signal generating section for the 1–6-MHz phase-lock loop.

(4) A stable 5-MHz clock signal (from which the 65, 70, 75, 80, 85, and 90 MHz harmonics are generated as reference frequencies) to the L.O. signal generating section for the six pump VCO bands.

c. Master Clock Signal Generator. The master clock signal generating section generates the 5-MHz master oscillator from which all of the reference and control frequencies are derived. The 100-kHz reference signal developed in the master clock section is used in the modulator section and in the control section. The other clock signals are used only as reference frequencies within the frequency synthesizer (A2).

d. Pump Signal Generator. The Hf VCO (pump) signal generating section receives frequency select inputs which are tuning control signals that cause selection of the appropriate Hf VCO band and mixer injection frequencies. Inputs from the master clock include the 5-MHz reference frequency and the 100-Hz signal used as an input to a ramp generator in the 1–6 MHz-VCO phase-lock loop. The Hf VCO (pump) output, a stable signal in the 88.999–61.000 MHz range, is routed to the RF translator (A1). A 90-MHz inject frequency is applied to the L.O. signal generating section for use in processing the L.O. RF signal. When the decoded tuning control signals are applied by the frequency select section, the pump tuning sequence is initiated. This causes the digital tune-in-progress (DTIP) signal to be routed (via the power supply section) to the mode and status panel (7A5/7A12).

e. L.O. Signal Generator. The L.O. signal generating section develops the L.O. signal for the RF translator (A1). Inputs are 100-Hz frequency select data from the frequency select section, a 90-MHz inject (reference) signal from the hf VCO signal generating section, and reference frequencies from the master clock signal generating section.

2–8. Power Supply Section
(fig. FO–5)

The power supply circuits generate the dc power required to operate the transmitter. A 120 Vac ±10% at 47 to 420 Hz is applied through fuse F301 to power supply A10 (+6.4 Vdc), A11 (+20 Vdc) and A19 (−28 Vdc). A +28 Vdc is applied through pin C of jack J4 to switch S301. When S301 is set to ON, the +28 Vdc enables relay K301. With K301 enabled, the return side of the 120 Vac is enabled through contacts on the relay. When this occurs, ac power is applied to A10, A11, A19. Power supply A19 is further protected by fuse F302. This is necessary because A19 is not regulated. With S301 set to ON, the 120 Vac is also applied through lamp DS301. When S301 is ON, DS301 illuminates to indicate ac power is applied to the power supply. The +28 Vdc regulated is also applied through S301 to the frequency synthesizer (A2). Contacts on a relay in the frequency synthesizer (A2) enable or open this +28 Vdc circuit. During the frequency synthesizer tuning cycle, the +28 Vdc is applied from the frequency synthesizer (A2) through contacts on K301 and S301 to the SYS TUNING indicator, which is physically located on the mode and status panel 7A5/7A12. With the +28 Vdc applied, the SYS TUNING indicator illuminates. At the end of the tuning cycle, the +28 Vdc circuit is opened and the SYS TUNING indicator is extinguished.

Section III. CIRCUIT ANALYSIS

2-9. General
(fig. FO-46)

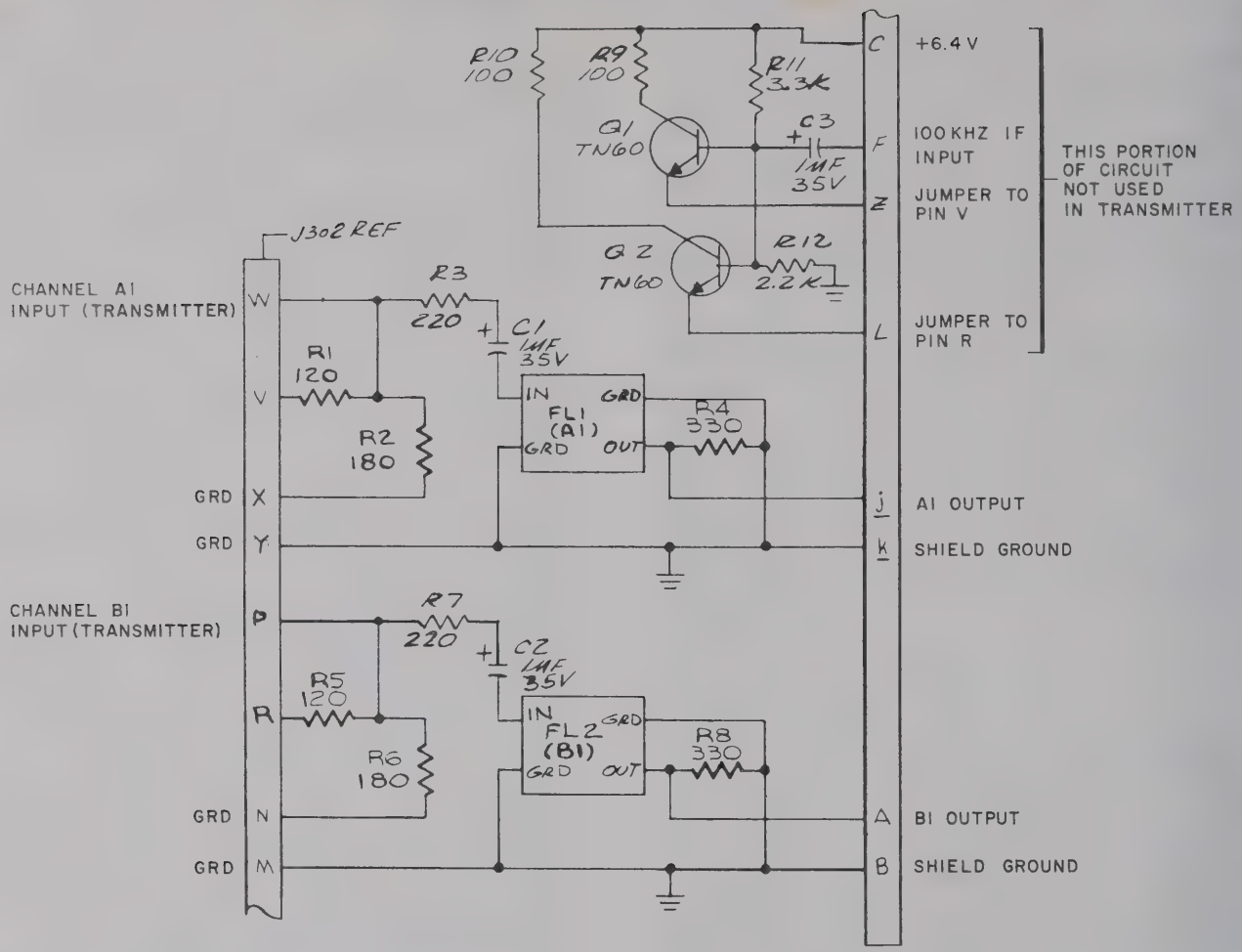
This section provides detailed theory of individual circuits in relation to the various wiring and schematic diagrams. These circuits are discussed with reference to physical location and detailed block diagrams. Figure FO-46 is provided, in lieu of an overall transmitter schematic to show interconnections as well as reference designation numbers (para 3-13), of the various assemblies, subassemblies, and modules described in this section. Each schematic diagram title also includes the reference designation number to identify the assembly, subassembly, or module shown. Where there is more than one production configuration, part numbers corresponding to the applicable configuration are also provided in the schematic diagram title. In many cases the differences between the various configurations is slight and only a single schematic diagram is required with the different configurations, identified with dash numbers, flagged on the schematic. If the differences are extensive, separate schematics are provided for both configurations.

2-10. Modulator Analysis

The modulator circuit consists of the dual balanced modulators (A7 and A21), the channel filter pairs (A3 and A6), and the multiplex carrier generator (A9). Each of the dual balanced modulators and each of the channel filter pairs serve one pair of channels (i.e., channels A1 and B1 or channels A2 and B2). Interconnection of these circuits within the transmitter unit are illustrated in figure FO-46.

a. Dual Balanced Modulator A7/A21. For this discussion of the dual balanced modulator (A7/A21), refer to figure FO-6. The dual balanced modulator for channels A1 and B1 (PC card A7) and for channels A2 and B2 (PC card A21) are identical, and this discussion is applicable to both units. Each of these dual balanced modulators contains two identical circuits; one circuit for channel A1 (A2) and one circuit for channel B1 (B2). The audio input information is supplied to pins H, J, and K of connector J301/J303, and is connected to the primary winding of transformer T1. The primary winding of transformer T1 is balanced and center-tapped, with an impedance of 600 ohms. A portion of the secondary winding of transformer T1 is then connected to jack J301/J303, for further connection to the MODULATION LEVEL A1 potentiometer on the front panel of the transmitter. The high side of the output is connected through a 47-ohm resistor to pin E of J301/J303, and the return is connected to pin F. (See insert on figure FO-6 for details of this connection.) The wiper of potentiometer R301 is connected back to J301/J303, pin T, furnishing the gain controlled level to the balanced modulator. Range of control by the MODULATION LEVEL A1 potentiometer is 0 dbm to +10 dbm. Pin T of connector J301/J303 is connected through capacitor C4 to the primary winding center tap of transformer T3. A 100-kHz carrier is applied to pin L of connector J301/J303, and is applied through capacitor C1 to the base of transistor amplifier Q1. The output of the amplifier is coupled to the primary winding of transformer T2. The secondary winding of transformer T2 is applied across the four diode ring modulator. Balanced modulation is accomplished in the ring modulator by enabling diode pairs CR1/CR2 and CR3/CR4 alternately at the carrier frequency rate (100 kHz), creating a low-impedance path to ground through each pair alternately. This signal path alternates through each half of the secondary winding of transformer T2, to the center-tap and to ground. This diode switching causes the audio to appear with alternating polarity across the secondary winding of transformer T3. This configuration also prevents the carrier signal from flowing through the primary of transformer T3, so it is not reflected to the secondary windings. The sideband energy is applied through emitter follower Q2 and capacitor C7 to pin R of connector J301/J303, which is then connected to the channel A1 input of the channel filter pair A1/B1 (A3) for further processing. The output of the balanced modulator is enabled by a ground-on-line channel enable signal applied to pin S of connector J301/J303, through diode CR5 to the emitter circuit of transistor Q2. The diode (CR5) in the channel enable line serves to isolate the circuit from any positive voltage which may be present on the channel enable input line.

b. Channel Filter Pairs A3/A6. Channel filter pairs for channels A1 and B1 (PC card A3), and for channels A2 and B2 (PC card A6), are identical circuits. Refer to figure 2-5 for card A3 and figure 2-6 for card A6 for this discussion. The double sideband suppressed carrier signal from the double balanced modulator is applied to pin W of the input jack for channel A1 (channel



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A3
   SECONDARY TRANSMITTER 6A11A3
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.

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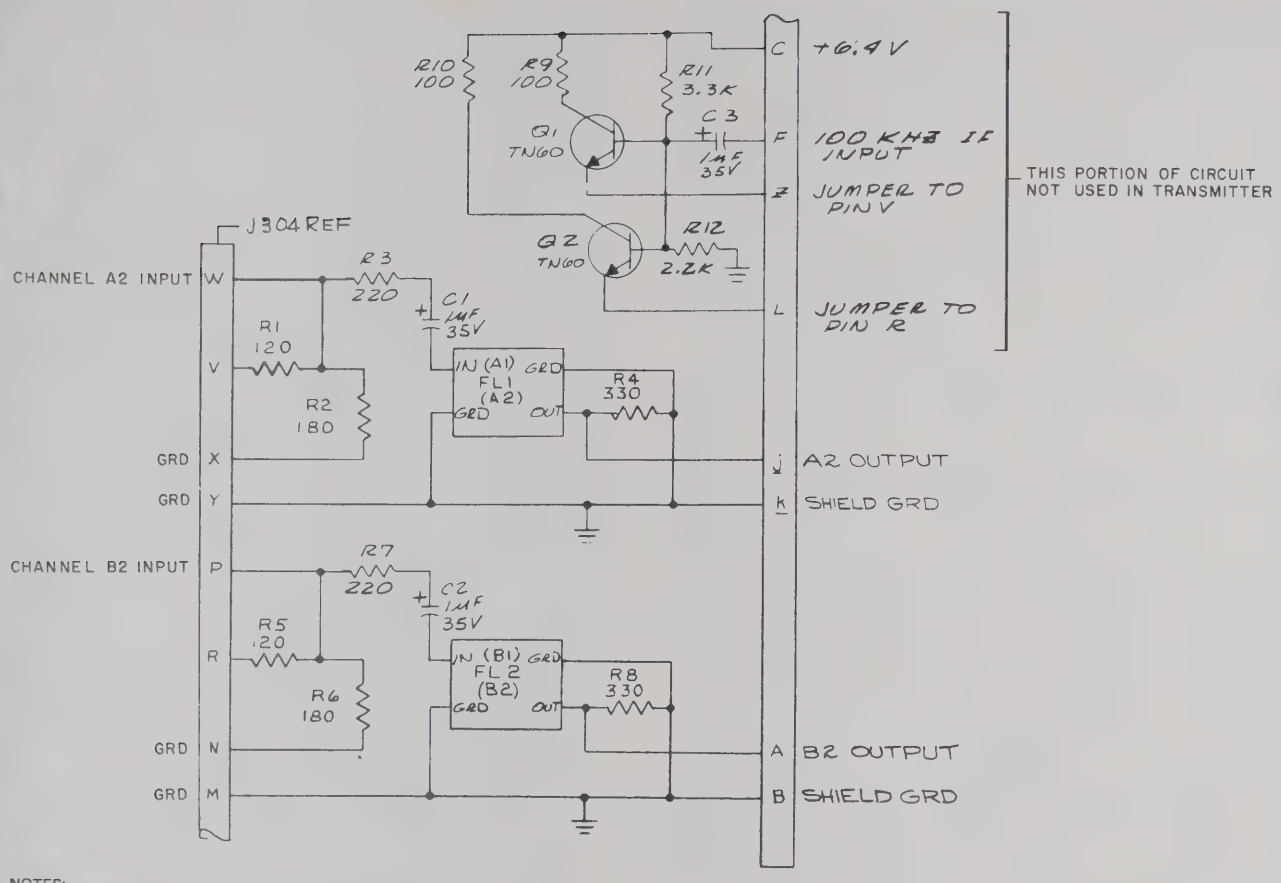
Figure 2–5. Channel A1/B1 filter pair (A3), schematic diagram.

A2), or to pin P of the input jack for channels B1 or B2. Each filter pair consists of two crystal filters FL1 and FL2, each of which has a nominal 3-kHz bandwidth, and are tuned to a specific passband in the 94- to 106-kHz range (depending on the channel). The channel A1 and B1 filters are tuned to pass the two inboard channels, located at 100.350 to 103.040 kHz for channel A1, and 96.960 to 99.650 kHz for channel B1. Similarly, the channel A2 filter frequency response is from 103.250 to 105.940 kHz, and the channel B2 filter frequency response is from 94.060 to 96.750 kHz. The resultant outputs of the channel filter pairs as independent sideband signals is coupled out on pin *j* for the A1 (A2) channel signal and on pin A for the B1 (B2) channel signal. These outputs are then coupled to the control circuits.

c. Multiplex Carrier Generator (A9). The multiplex carrier generator (A9) (fig. 2–7) provides two stable frequencies used as injection reference signals for the channel A2–B2 dual balanced modulators. These signals provide multiplex sideband frequencies above and below the 100-kHz (nominal) carrier signal. Each circuit is basically a crystal controlled Butler oscillator consisting of crystal (Y1A) and feedback amplifier Q1, with an emitter follower output stage Q2. Both oscillators are identical except for the crystal frequency output; channel B2 generates



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A6
   SECONDARY TRANSMITTER 6A11A6
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.

EL5895-356-34-1/8-7

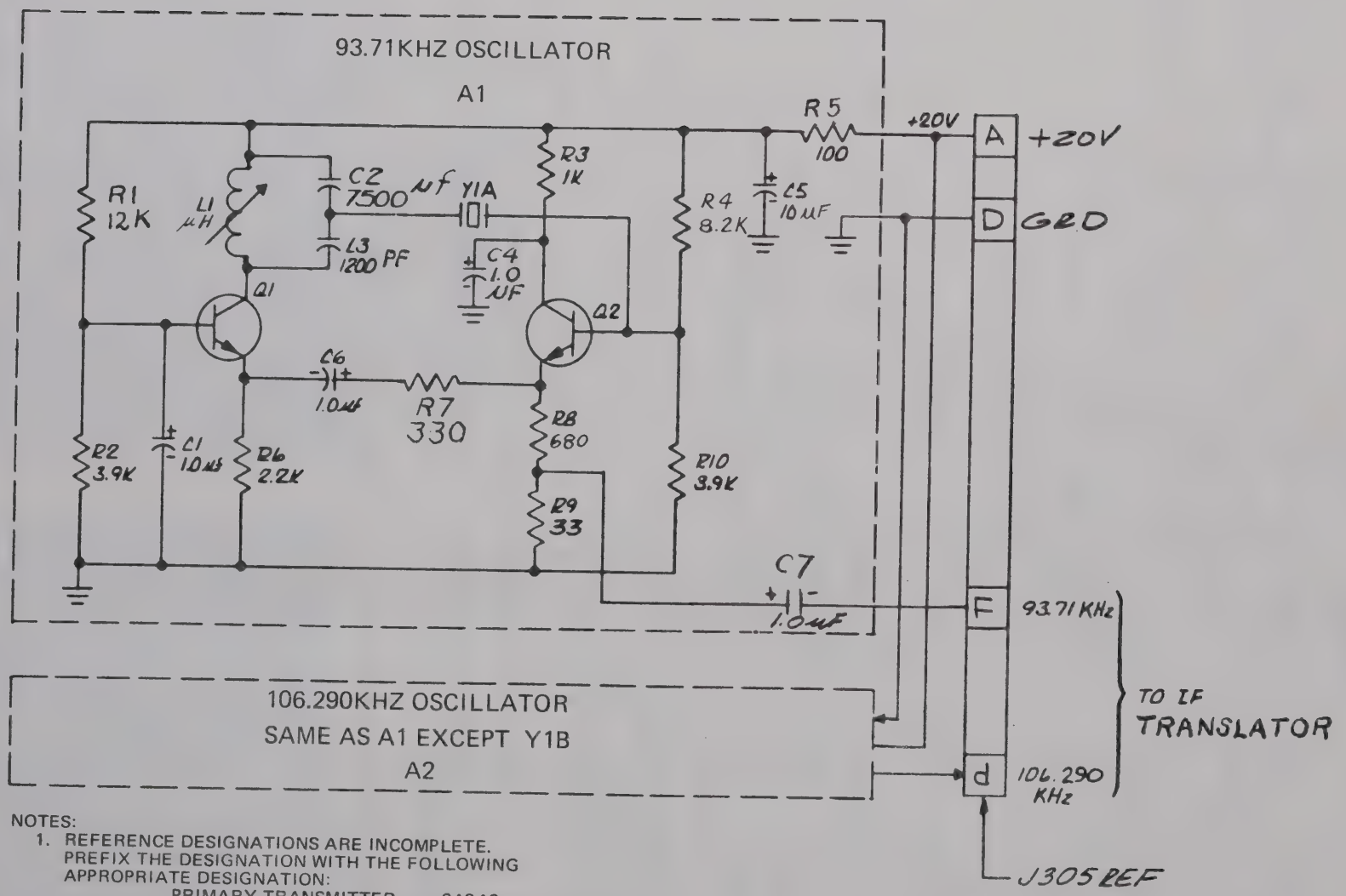
Figure 2–6. Channel A2/B2 filter pair (A6), schematic diagram.

a 93.71-kHz signal frequency and channel A2 a 106.29-kHz signal frequency.

2–11. Control Analysis
(fig. FO–7)

The transmitter control circuits consists of signal control module A5, transmit gain control module A4, and automatic channel loading module A8. In addition, the control circuits also include components mounted on the transmitter front panel. Since the setting of the front panel controls interact with the three modules stated above, the front panel controls will be discussed first. The front panel controls can be divided into three functional categories: those associated with the modulator, the power supply, and the control circuits. Those controls associated with the modulator and the power supplies are not discussed in this section since they are discussed separately with the sections covering the modulator and the power supplies sections: refer to paragraphs 2–10 and 2–15 respectively.

a. Front Panel Controls. The front panel controls associated with the control circuits are the CARRIER ADJUST switch (S303), CARRIER ADJUST LOCAL STEP (−db) switch (S302), CARRIER ADJUST CONT. potentiometer (R-305), TGC VOLTAGE test point (TP301), and the EXCITER GAIN control (R318). The CARRIER ADJUST switch (S303) controls the transmitter operating mode selection and output signal level. In the STEP position of S303 the transmitter operates in the ISB mode and the signal derived from the CARRIER ADJUST LOCAL STEP (dB) switch (S302) controls the output signal level of the transmitter in 3-db steps. In the CONT. position of S303, the transmitter operates in the ISB mode and the CARRIER ADJUST CONT. potentiometer (R305) controls the output signal level of the transmit-



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A9
   SECONDARY TRANSMITTER 6A11A9
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. ALL TRANSISTORS ARE 2N2222.

EL5895-356-34-1/8-8

Figure 2-7. Multiplex carrier generator (A9), schematic diagram.

ter. In the AM position of S303, the carrier level (AM) potentiometer A5R66 sets the required carrier level for AM operation. The primary switching elements to accomplish operating mode and carrier selections are switch S303, and tune enable relay K302 (shown in the deenergized state). There are basically two modes of operation: manual and automatic (tune enable). In manual operation, mode selection is controlled by switches and potentiometers on the transmitter front panel and/or the mode and status panel (7A5/7A12). The automatic mode is under control of the external linear power amplifier (LPA), and is used only to provide a signal to the LPA during its tuneup. In manual operation, the transmitter is keyed on and off by a transmitter keying signal (ground) applied from the mode and status panel (7A5/7A12) except in compatible AM operation. In compatible AM, the carrier insertion depends upon whether a carrier enable signal (ground) is applied from the mode and status panel (7A5/7A12). With a carrier enable signal applied, switch S303 determines which element controls the carrier level as previously described. With S303 in the STEP position, the carrier level is controlled by the position of the CARRIER ADJUST LOCAL–STEP (−db) switch (S302), and step attenuator R307 through R317. With switch S303 in the CONT position, the carrier level is controlled by the position of the CARRIER ADJUST-CONT. potentiometer (R305). In the REMOTE position of switch S303, the carrier level is set by a dc level adjusted at the mode and status panel (7A5/7A12). In the AM position (the only manual mode of operation which does not require a separately supplied carrier enable signal), switch S303B provides the ground for a carrier enable signal. In this mode the carrier is set to a predetermined level by the carrier level (AM) potentiometer A5R66. The automatic mode is only used during tuneup of the external LPA. When a change is made in the frequency of the transmitter, the LPA will, in most instances, require retuning. The transmitter supplies a signal at the desired output frequency to the input to the LPA. The digital tune enable (DTE) signal is applied simultaneously to both the transmitter and the LPA. With the DTE applied to the LPA, a ground level tuning signal (tune enable) is sent to the transmitter. This signal causes relays A5K1, K302, and A8K1 to be energized. The modulation disable relay A5K1 interrupts the modulation products (independent sidebands) which are normally supplied to the signal amplifier circuit (transistors A5Q4 through A5Q7). This action insures that the signal supplied to the RF translator (A1) will contain no modulation products which might interfere with the tuning process. When the tune enable relay (K302) is energized, the following actions occur simultaneously:

(1) Control of the carrier level is removed from the selection by switch S303A, and the carrier level is controlled by the setting of the tune control potentiometer (A5R71) located on the signal control module A5.

(2) A ground potential applied through contacts 6 and 7 of tune enable relay K302 keys the transmitter.

(3) The carrier amplifier is enabled by a ground applied through contacts 9 and 10 of relay K302.

(4) The TGC voltage is clamped to a predetermined level. This is accomplished by applying a ground through contacts 15 and 16 of relay K302, which resets and holds the TGC memory circuits at a fixed value.

(*a*) The ultimate result of all of these actions is that a fixed-level, carrier only signal at the desired output frequency is supplied to the input of the LPA from the output of the transmitter. When the tuning of the LPA is complete, the tune enable signal is no longer present, and the transmitter circuits return to the operational mode which was previously selected by the manual controls.

(*b*) The tune enable (automatic) mode also uses a tune leveler circuit to produce a constant transmitter output level during LPA tuning. During the initial portion of the LPA tuning cycle, the LPA operates below rated power. As the LPA tunes to frequency, the power level is increased to the rated output. If the TGC circuit remains unchanged during the initial tuning phase, the gain of the transmitter would be increased to a maximum in an effort to obtain rated output. If the gain of the LPA is increased during the final portion of the tuning cycle, the LPA may then be overdriven by the transmitter output before the TGC circuit is able to react to the gain change. Thus, during tune enable mode, the TGC voltage is held at a fixed value by the TGC memory reset signal applied through K302. However, another gain control circuit is required to compensate for the differences in transmitter gain at various points in the tuning range. This is the function of the tune leveler circuit, which is active only during the tune enable mode. The third

relay (A8K1) activated by the tune enable signal, causes a fixed-level voltage to be applied to the base of A8Q4. This fixed signal overrides the TGC voltage which in turn fixes the gain of the AGC'd amplifier A1A2Q4 in the RF translator (A1). Simultaneously, relay A8K1 completes a circuit between the ACL circuits and signal amplifier gain control transistor (an FET) A5Q6. The signal from the ACL is a dc level which has been derived from a detector circuit in the RF translator (A1). This detector samples the transmitter output level. Thus, the output level sample signal is fed back to control the gain of signal amplifier transistors A5Q4, A5Q5, and A5-Q7, effectively maintaining the transmitter output at a constant level. After completion of tuning in the LPA, relay A8K1 is restored, and the operation of the gain loops return to normal.

(*c*) The EXCITER GAIN control, potentiometer R318 controls the operating bias voltage on transistor A8Q4 located in the ACL PC card. Varying the gain of this transistor stage varies the level of the AGC voltage supplied to transistor A1A2Q4 in the RF translator (A1), which in turn controls the gain of that transistor stage. This, in turn, controls the level of the output signal from the transmitter.

b. Signal Control A5 PC Card. The signal control A5 PC card (fig. FO–8) receives the four ISB signals from the channel filter pairs in the modulator circuits, a tuning control signal from the ACL module (A8), a 100-kHz signal from the frequency synthesizer (A2), and various control signals from the external LPA and from the transmitter front panel controls. The four independent sideband signals from the channel filter pairs in the modulator circuits are applied to the multiplex combiner circuit, which is a resistive combiner network consisting of resistors R1, R2, R3, and R4. The composite audio signal resulting from the combining action is fed to the ACL PC card A8, through connector J306 pin W. The signal is scaled in the ACL PC card. The signal returned to the signal control PC card from the ACL PC card is maintained at a constant level regardless of the number of channels enabled through the action of the ACL PC card. This returned signal is applied to the signal control A5 PC card through connector J306 pin U. This multiplexed, gain controlled signal from the ALC module is then applied to a two-stage amplifier consisting of transistors Q1 and Q3. The overall gain of these transistor amplifier stages are in turn controlled by a gain signal developed within the ALC PC card A8. Thermistor R79 in the emitter circuit of transistor Q3 provides temperature compensation of the gain of Q3 by controlling the degenerative feedback loop of the stage. Field-effect transistor Q2 acts a voltage controlled resistor in the emitter circuit circuit of transistor Q1, controlling the degenerative feedback in accordance with the applied ALC sample voltage supplied from the LPA. This sample voltage is a dc signal in the range of 0 to −10 Vdc, which varies with the peaks of the modulation envelope which exceed the rated output of the LPA. This ALC sample voltage is applied to the base of transistor Q8, which inverts the signal and applies it as a positive voltage to the gate terminal of FET Q2. The gain of transistor stage Q1 is controlled by the source-to-drain impedance of FET Q2. Thus, an increase in the voltage at the gate of FET Q2 creates a corresponding increase in this impedance, which in turn increases the degenerative feedback for transistor Q1. Changes in this gain are reflected in the peak ISB level supplied to the LPA from the transmitter, and thus control the transmitter sideband output level. The ALC loop time constants are controlled by the network composed of diode CR2, and resistors R38, R39, R40, and capacitor C16. If the ALC sample voltage at the base of transistor Q8 increases in a negative direction, diode CR2 becomes forward-biased, and capacitor C16 becomes charged through resistors R38, R39, and R40 and diode CR2. The attack time of the loop is thus approximately 4 ms. The discharge path for capacitor C16 is through resistor R40, providing a release time constant of 120 ms.

(1) ALC sensitivity adjust potentiometer R39 in the Q8 collector circuit sets the threshold sensitivity of the ALC loop. The operating bias at the Q2 source is determined by ALC calibrate potentiometer R10.

(2) ALC ON/OFF switch S1 permits disabling the ALC loop. With S1 in the off position, the level at the Q2 gate is established by potentiometer R41, capacitor C17, and associated circuits. Potentiometer R41 is adjusted to provide the same output level as is present at R39 when the transmitter provides rated output.

(3) The output of ALC'd amplifier Q1 Q8 is applied through the contacts of modulation disable relay K1 to the base of emitter follower Q4. Relay K1 is energized only when the transmitter is being used as a signal source for tuning the LPA (in the tune enable mode). At this time

the ISB signal line is interrupted and a low-pass series circuit R72–C38 shunts to ground any audio appearing at the Q4 base. When the LPA tuning cycle is completed, the tune enable (ground) is removed from J306–J and the output of transistors Q3 is again applied to Q4.

(4) The base circuit of Q4 is also used as a summing point for the 100-kHz carrier insertion with the ISB signal. The 100-kHz signal from the frequency synthesizer (A2) is applied to the signal control A5 PC card through J306–e to the base of carrier amplifier Q9. Transistor Q9 is switched on when a carrier enable signal (ground) is applied through J306–c. The carrier enable signal is applied from a control on the mode and status panel (7A5/7A12), via CARRIER SELECT switch S303B on the transmitter front panel when it is in the AM position, and/or tune enable relay K302 when it is energized during the tune enable mode. The carrier enable signal overcomes the positive voltage applied to the Q9 emitter by voltage divider R52–R53. The gain of Q9 is controlled by the voltage level applied through J306–d. During LPA tuning (tune enable mode) this level is set by tune control potentiometer R71. At other times this level is determined by the element selected by transmitter front panel switch S303A. In the REMOTE position the level is controlled from the mode and status panel (7A5/7A12). In STEP or CONT position, it is controlled by the related front panel controls; and in AM position it is controlled by AM potentiometer R66. The signal at the output of Q9 is coupled through C20 and R57 to the Q4 base. Q4 is an emitter follower which drives signal amplifier Q5 and its output stage, Q7. The Q4 output is also applied to Q10 for processing in the TGC loop.

(*a*) The Q4 output to TGC reference amplifier Q10–Q11 represents the overall input signal level to the transmitter, either ISB or carrier, or a combination of both. After processing, it is compared with a sample of the LPA output to measure the gain of the transmitter-LPA combination. The first step in processing is amplification through Q10 and Q11. Circuit components C35, R75, C28, and L2 in the Q11 collector peak the response of the stage at 100 kHz. Transistor Q11 drives a detector circuit consisting of CR4, R74 and C29. The negative voltage thus developed is applied through low-pass filter L3, C30, and L4, and J306–Z to the TGC differential amplifier on the TGC card A4. As explained below, the TGC reference amplifier is switched off when the transmitter is not keyed. The time constant of the TGC reference circuit is determined by R70, C40, and C41.

(*b*) The Q4 output level to signal amplifier Q5–Q7 is established by exciter gain control potentiometer R69. The gain of Q5 is controlled by the TGC voltage. After comparison of the TGC reference signal and the TGC sample from the LPA, a TGC voltage is developed which is a level between 0.5 and +3.5 Vdc and is fed back through J306–a to the gate of FET Q6. Q6 operates in a similar manner as Q2 in the ALC circuit. The drain-to-source resistance of Q6 varies with the TGC voltage and changes the degenerative feedback in the Q5 stage. As the voltage of the FET gate is increased, the degenerative feedback is increased and the gain of Q5 reduced. Potentiometer R34 sets the threshold for Q6 operation and potentiometer R26 sets the operating bias for the Q6 source.

(5) During the tune enable mode, the gain of Q5 is controlled by the tune leveler signal applied through J306–Y. This signal is derived from the detected RF translator (A1) output via dc amplifiers and relay A8K1 on the ACL PC card. The tune leveler signal overrides all other signals at the Q6 gate, thus controlling the Q5 gain. When the transmitter is not in the tune enable mode, the input through J306–Y is disconnected.

(6) Signal amplifier Q5–Q7 and TGC reference amplifier Q10–Q11 are switched on by the transmitter key signal applied through J306–b. During tune enable mode this signal is applied from K302. At all other times it is supplied from the mode and status panel (7A5/7A12) in order to enable the transmitter output. The enable signal is a ground applied to the junction of R30–R31 in the Q7 emitter. Transistor Q7 is then forward-biased and conducts, supplying an output to pin j. When the ground signal is not present, Q7 is biased off and no output is available from the signal amplifier. With no keying signal applied, modulation and/or carrier signals may still be available at the Q4 output. This could cause an unbalance in the TGC differential amplifier if the TGC reference output was not simultaneously disabled. Thus when the transmitter key signal is not applied, the relatively high potential at the junction of voltage divider R31–R32 is fed through R61 to the emitter of Q10, disabling this input stage. When the transmitter is keyed, the ground through J306–b switches on Q10 and allows the TGC reference amplifier circuit to operate.

(7) The signal control A5 PC card also contains a −20 Vdc regulator circuit whose output is used within the board and externally by the TGC PC card A4, ACL PC card A8, and the frequency synthesizer (A2). Transistors Q12, Q14, and Q13 provide a regulated −20-volt output which is applied to external circuits through J306–H. The −28-volt unregulated input is applied through J306–C. A sample of the regulated output is fed back to the base of Q13 through voltage divider R77, R76, and R78. In transistor stage Q13 this sample is compared with a −10 Vdc reference level supplied to the Q13 emitter from zener diode CR3. As the −20 Vdc output level tries to change, the conduction of Q13 is varied. This variation is fed through emitter follower Q14 to change the conduction of series regulator Q12 in a direction to counteract the originating change in the −20 Vdc output. Potentiometer R76 sets the operating level of the regulator.

c. Transmit Gain Control (TGC) PC Card A4. The TGC PC card (fig. FO–9) consists of a TGC differential amplifier, TGC memory with associated control circuits, and a digital-analog (D–A) converter. In addition, the card contains a reset generator which operates in conjunction with the frequency select circuits. The TGC differential amplifier, consisting of transistor stages Q3 and Q4 compares a sample voltage supplied from the TGC reference circuit in the signal control A5 PC card with a sample of the LPA output to determine the overall gain of the transmitter/LPA combination. If the gain is not equal to a predetermined value, a positive or a negative error signal is established which updates the TGC memory. The TGC reference signal is applied to the differential amplifier through connector J307 pin d, and then coupled to the base of transistor Q3 via emitter follower stage Q1. A dc-sample voltage from the LPA is applied to the differential amplifier through connector J307 pin h. The level of the sample input is within the range of 0 to −10 Vdc. The sample voltage is then scaled by potentiometer R5 and coupled to the base of Q4 through emitter follower Q6. Transistor Q7 is the constant-current source for the differential amplifier. The amplifier outputs are coupled through emitter followers Q2 and Q5 and applied to the bases of Q9 and Q10 respectively. These stages in turn are drivers for gates Q8 and Q11. Diodes CR1 and CR2 prevent excessive back-biasing of the base-emitter junctions of Q8 and Q11. The operation of the differential amplifier and the gates it controls are discussed in detail below in relationship to the TGC memory add and subtract sequences.

(1) The TGC memory is a five-stage ripple counter which can count either forward or backward. Stored in the counter is a digitial value representative of the gain of the transmitter at any given time. The outputs of gating transistors Q8 and Q11 are used to control the add and subtract gates of the TGC memory bank. The add gates are G1C, G1D, G2C, G2D, and G3D. The subtract gates are G1A, G1B, G2A, G2B, and G3A. The memory consists of five identical flip-flops; FF1 through FF5. A negative-going transition from +4 to 0 Vdc at the C (clock) input causes the flip-flop to change state. The flip-flop circuits are such that a low level at the S (set) input sets the flip-flop to the one state, in which the Q output is high and the $\overline{Q}$ is low. A low input at R (reset) will reset the flip-flop to zero (Q low, $\overline{Q}$ high). For an add sequence the counter uses the $\overline{Q}$ outputs; for subtract, the Q outputs.

(*a*) Driving the memory is a low frequency astable multivibrator composed of transistors Q13 and Q14. The multivibrator operates at between 8 and 10 Hz, the exact frequency being noncritical. The flip-flops form a bidirectional counter that can count up to 32. The counter reset state is represented by ones in flip-flops FF3, FF4, and FF5, and zeroes in flip-flops FF1 and FF2. The counter assumes this state when the reset signal (a ground potential from the tune enable relay) is applied through J307–Z to the set inputs of FF3, FF4, and FF5, and to the reset inputs of FF1 and FF2. In the reset state, the number in the counter is 00111, reading from the least significant digit on the left to the most significant on the right.

NOTE

The relative positions of the least and most significant digits read out by the counter are determined by the arrangement of the flip-flops and the order in which they change state. Flip-flop FF1, which corresponds to the least significant digit, receives the clock pulse from the multivibrator through the first gating circuit. Flip-flop FF5, the most significant digit, receives its input clock pulse from the last gating circuit. Thus, in the notation of any given sequence, the lowest or least significant

digit appears at the left and the highest or most significant digit at the right.

(*b*) Looking at the add sequence and assuming that the counter is at (16), the flip-flops would be in the state represented by 00001. The counting sequence is initiated by an input signal at J307–h, which causes an unbalance of the differential amplifier. If the TGC sample (representing the level at the output of the LPA) is higher (more negative) then it should be for the level of the signal supplied to the transmitter gain-controlled stages (represented by the TGC reference signal), the differential amplifier is unbalanced in a direction to cause Q5 to conduct more than Q2. This turns off amplifier Q10 and its output is sufficient to cause cutoff of gating transistor Q11. The high output of Q11 enables all of the add gates. When the G1D add gate is enabled, the clock pulse is passed to FF1 causing it to change state. When FF1 assumes the one condition, it produces a low output through $\overline{Q}$ to the input of G1C. A low G1C causes the G1C output to go high, and FF2 does not change state. Since the flip-flop acts as a ripple counter, with each stage dependent upon changes in the previous stage if FF2 does not change state, none of the subsequent flip-flops will change. Therefore, the word in the counter becomes 10001. The next clock pulse causes FF1 to again change back to the zero state, so that its Q output goes high. Now there are two high inputs at G1C, resulting in a negative going output which is applied to the clock input of FF2 and causes it to change state. Flip-flop FF2 will now assume the one state since it was previously in the zero state; however, the $\overline{Q}$ output of FF2 will now go low, causing the G2D output to go high and FF3 does not change state at this ime. The word now read into the counter is 01001, from the least significant to the most significant number. It should be noted that with each pulse, the counter assumes a higher count.

(*c*) The next clock pulse, again through G1D, causes FF1 again to change state. When FF1 goes to a one, its $\overline{Q}$ output goes low. A low input to G1C causes its output to go high. This prevents a negative pulse into FF2. Since FF2 does not change state, all the flip-flops following it will not change state. Therefore, the count will now be 11001.

(*d*) If the add condition still exists, the next clock pulse will go through G1D causing FF1 to change state again. When FF1 goes to the zero (reset) state, its $\overline{Q}$ output will then go high. A high input to G2D will cause a low output which is fed as a clock pulse to FF3. Since FF3 was in the zero state, it will now go to the one state. The $\overline{Q}$, output of FF3 will now go low, and a low input to G2C will produce a positive G2C output. Flip-flop FF4 does not change state and remains in the zero state. Therefore, FF5 remains in a one state and the counter now reads 00101. The next clock pulse from G1D to FF1 causes it to change from zero to one. The resulting low $\overline{Q}$ output is applied to G1C, causing the G1C output to go high. Flip-flop FF2 does not respond to a clock pulse input so it remains in the zero state and the counter now reads 10101. Similarly, for the next clock pulse, the counter reads the next state counted up (01101) and so on.

(*e*) The subtract sequence is similar to the add except that the flip-flop outputs steered to the subtract gates are taken from the Q terminals. Assume that the counter has the number 00101 (20) inserted, and that the subtract mode exists due to the application of a Q2 output to amplifier Q9 and gating transistor Q8. In this case the Q8 output is high; subtract gates, G1A, G1B, G2A, G2B, and A3A are enabled, and the add gates are disabled. The next clock pulse through G1A causes FF1 to change from the zero to the one state. In the one state, the Q output of FF1 is high, and is fed to G1B to produce a low output clock pulse to FF2. The pulse causes FF2 to change from the zero to the one state. The Q output of FF2 in the one state is high, and causes the G2A output to go low, feeding a clock pulse to FF3. Since FF3 was in the one state originally, it now goes into the zero state. The Q output to G2B is now low which causes the G2B output to go high, but the high at the input to FF4 has no effect at this time. Consequently, the word in the counter is 11001 (19), reading from the least significant to the most significant digit. The net result is that the counter has counted back one count.

(*f*) In the same manner, the next pulse will cause FF1 again to change state, but since going from the one to the zero state causes the Q output to go low, the low input to G1B results in a high output from G1B, which has no effect on FF2. Because FF2 does not change state, no other stage changes state and the new count is 01001. Thus, the counter has counted back one step again. As long as the subtract gates are energized, the counter will continue to count backward (subtract). When neither the add nor the subtract signals are applied, the differential amplifier is in balance and neither Q8 nor Q11 will

produce an output. As a result, neither the add nor the subtract gates will be energized, and no clock pulses will be fed to FF1. Therefore, the counter will remain in the last previous state.

(2) The D–A converter consists of a set of weighting resistors which operate from the voltages derived from the Q outputs of all of the flip-flops. These voltages at the Q outputs are clamped to a temperature-stabilized level by CR-10, CR3 through CR6, and CR12. The output is summed through weighting resistors R36 through R40. The weighting is such that the most significant digit has the most effect. The sum of these voltages is supplied through J307–X as the D–A output.

(3) The reset generator for the frequency select memories is also located on the TGC PC card A4. Action is initiated when the digital tune enable (DTE) signal (a momentary ground) is supplied from the frequency select panel (7A4/7A11). The DTE signal, applied through connector J307 pin P performs two functions:

(*a*) It is routed through diode CR14 and connector J307 pin M to provide the DTE signal to the in-lock detector circuit (A2A3A3) in the frequency synthesizer (A2). This initiates the digital-tune-in-progress indication signal which is applied to the mode and status panel (7A5/7A12).

(*b*) It is applied through diode CR13 to trigger the reset generator composed of transistors Q17, Q18, and Q16. Transistors Q16 and Q17 are configured as a one-shot multivibrator, which develops a 40-ms pulse having the required rise time and delay characteristics. The output of the one-shot multivibrator is coupled via transistor Q18 to connector J307 pin V, and resets all sections of the frequency select memory, and allows the frequency information from the frequency select panel (7A4/7A11) to be read in to the frequency select memory circuits. A voltage regulator circuit supplies the −5 Vdc to the reset generator. In the −2 configuration of the equipment, this consists of a Zener diode, CR11, resistor R44 and capacitor C15. In the −1 configuration of the equipment, transistor Q15 is added in an emitter-follower configuration (para 3–9*e*(3)).

d. Automatic Channel Loading (ACL) PC Card A8. The automatic channel loading (ACL) PC card A8 (fig. FO–10) contains the ACL amplifier and the tune leveler circuit. The ISB signal from the multiplexer on the signal control PC card A5 is supplied through connector J314 pin P to the base of transistor Q2. The collector output of transistor Q2 is connected to four parallel-connected attenuator networks. The attenuator networks are then connected to the four channel enable ground-on-line switching circuits. The channel enable circuits effectively function as a variable impedance for the output of transistor Q2. As each enable circuit is switched on at the mode and status panel (7A5/7A12), the signal across resistor R7 is varied accordingly. The resultant output for any combination of channels enabled will be a fixed-level signal applied through capacitor C2 and connector J314 pin L to the amplifiers on signal control PC card A5. The tune leveler circuits contained on the automatic channel loading PC card A8 create a loop with circuits on other cards. This loop is shown in the tune leveler circuits, simplified schematic diagram (figure FO–11). Associated with the tune leveler circuits are the NORMAL LEVELS METER on the mode and status panel (7A5/7A12), the tune leveler gain control loop, and the EXCITER GAIN control potentiometer located on the transmitter front panel. The input to the remote RF indicator circuit is the rectified, filtered output from the video amplifier portion of the RF translator (A1). This signal is applied to input amplifier transistor Q1 (shown in figure FO–10) for scaling and isolation. It is then routed as an emitter output from transistor Q1 through connector J314 pin C to the indicator circuit. The amplitude of the signal varies directly as the RF signal level at the transmitter output varies, and provides a valid indication of the actual RF level. Diode CR6 is a temperature-compensating element utilized to compensate for variations in the base-emitter junction voltage of transistor Q1.

(1) The tune leveler circuit is active only during the LPA tuning cycle. The same detected output of the RF translator (A1) which is applied to transistor Q1 for an RF indicator signal is also utilized for the input to the tune leveler circuit. However, the output is taken from the collector of transistor Q1 for tune leveling. This signal is coupled to the base of dc amplifier transistor Q3, whose emitter bias is controlled by potentiometer R14. When the tune enable signal is present, relay K1 becomes energized and the signal is routed to the signal amplifier circuit on signal control PC card A5, where it overrides the TGC voltage. Tune level potentiometer R14 permits finite adjustment of the transmitter output over the range of 2 to 4 volts rms. When not in the tune enable mode, relay K1 is deenergized, and the signal amplifier is again under control of the TGC circuit.

(2) Dc amplifier transistor Q4 controls the gain of RF translator (A1). During tuning of the LPA, the tune enable signal energizes relay K1, thereby applying a fixed voltage level to the base of transistor Q4 from the junction of resistors R16 and R17. This voltage overrides all other input signals to transistor Q4, and produces a constant output signal to RF translator (A1). At all other times, the output of transistor Q4 is dependent upon a combination of inputs from the EXCITER GAIN control R318 and the TGC voltage supplied from the TGC digital to analog (D–A) converter. The EXCITER GAIN potentiometer (R318) extends the control range of the TGC loop to compensate for gain variations in the transmitter and the power amplifier due to aging and for different power output setting required by the user. The gain control circuits include an emitter-follower stage (transistor Q4) on the ACL card, the 5-kohm potentiometer (R-318) on the transmitter front panel, and the AGC amplifier transistor Q4 in the RF translator (A1). Since potentiometer R318 is a calibration control rather than an operating control, it is fitted with a locking nut to prevent inadvertent change in the potentiometer setting. Except in the tune enable mode, the bias at the base of transistor Q4 is determined by the setting of EXCITER GAIN potentiometer (R318), which can be varied manually to create a change of 2 volts at the base of transistor Q4. The bias is also affected by the TGC voltage which has a dynamic range from 0.5 volt to 4 volts. Thus, the overall range provided by the combined control action is approximately 6 volts. The output of transistor Q4 is coupled to the 91-MHz IF amplifier in the RF translator (A1). In the tune enable mode, the +2 volts furnished by the voltage divider composed of resistors R16 and R17 is applied to the base of transistor Q4 through the closed contacts of relay K1. This voltage level overrides the voltage level from EXCITER GAIN control (R318) and the TGC memory inputs so that the gain of AGC amplifier, transistor Q4 remains at maximum.

2–12. Rf Translator A1 Analysis

The RF translator A1 circuits consist of a converter (A1A2), low-pass filter assembly (A1A5), preamplifier (A1A1), video amplifier (A1A3), filter box (A1A4), and a −7 Vdc voltage regulator (A1A6). Internal connections within the rf translator (A1) are shown in figure FO–48.

a. Converter Assembly A1A2. Two versions of the converter assembly (A1A2) are available, and may appear in the equipment. One, designated as 233–20–255, is shown schematically in figure FO–12. The second version, designated as 233–20–262, is shown schematically in figure FO–13. The two converter assemblies are physically and electrically interchangeable in the RF translator (A1). Differences between the two converter assemblies are discussed below.

(1) In the 233–30–255 version of the converter, a nominal 100-kHz signal from the control circuits is applied through connector J5102. This signal may be a modulated signal (i.e., carrying one or more of the independent sidebands) or it may be only the basic 100-kHz carrier. This signal is coupled through A T-filter to the base of transistor Q1, which is the first mixer stage in the converter. A nominal 90.9-MHz signal (L.O. signal) is applied to connector J5104, amplified by transistor Q2, and coupled through stepdown transformer T2 to the emitter of the mixer transistor Q1 as the second input. A tuned crystal filter consisting of crystal Y1 and capacitor C12 in the output (collector) of transistor mixer Q1 serves to attenuate any 90.9-MHz components which might otherwise appear in the output of the mixer circuit.

(2) In the 233–20–262 version of the converter, the first mixer, consisting of the input T-filter network, transistor Q1, transformer T1, and crystal filter Y1 and C12 are replaced with an integrated circuit double balanced mixer.

(3) The output signal from the first mixer is transformer-coupled through transformer T1 to the input of a 91-MHz bandpass filter. The bandwidth of the bandpass filter is a nominal 20 kHz. The IF signal output of the bandpass filter is coupled through resistor R37 to the base of AGC controlled amplifier, transistor Q4.

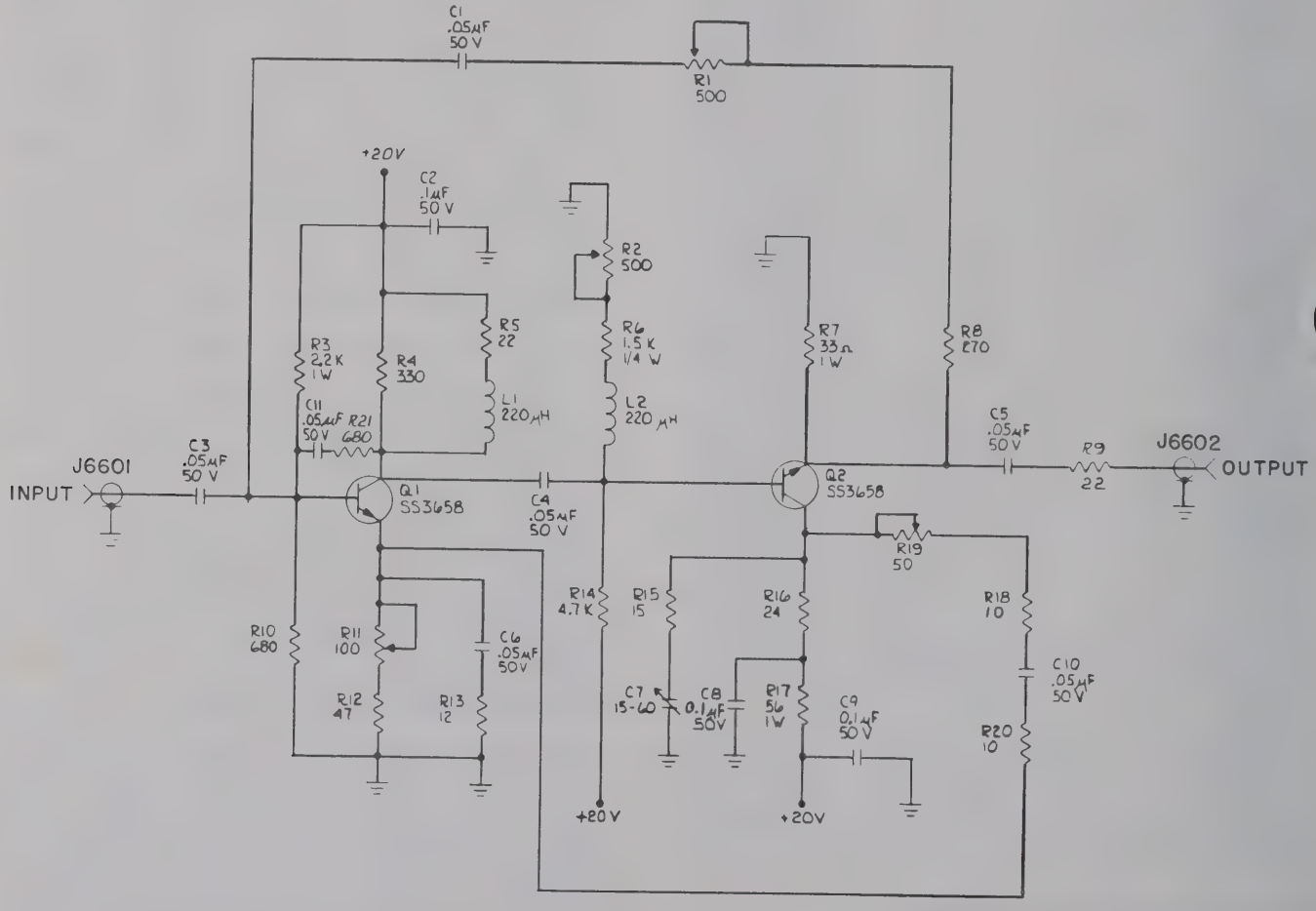
(4) Transistor Q4 is the AGC'd 91-MHz amplifier stage. Zener diode CR3 and resistor R39 in the emitter circuit of transistor Q4 serve to temperature compensate the −5 Vdc emitter supply voltage for the stage. Further temperature compensation and gain stabilization for transistor Q4 is furnished by the action of transistor Q5 and the associated circuitry. AGC is applied to the amplifier base circuit of transistor Q4, which will serve to determine the overall gain of the amplifier stage. Variable inductor T3 in the collector (output) of transistor Q4 is adjusted for maximum signal transfer at a frequency of 91 MHz. The output of the AGC'd stage is coupled

across capacitor C47 to the primary of transformer T4 in the balanced mixer circuit.

(5) The second input to the balanced mixer circuit is the pump signal (61.000 to 88.999 MHz) from the frequency synthesizer (A2), which is applied from connector J5103, and buffer amplified in transistor stage Q3. The output of the buffer amplifier is applied to the balanced mixer through a center-tap in the secondary of transformer T4. The balanced mixer, which is of the two-diode type, substantially reduces the L.O. frequency components, and provides rejection of even-order harmonics at the output. The resultant signal, consisting of ISB channels centered about the selected frequency in the 2–30-MHz range is coupled across resistor R25 to connector J5105, and to the low-pass filter assembly.

b. Low-Pass Filter A1A5. The low-pass filter assembly (fig. FO–14) is a two-section, multipole, tuned L–C array. Signals between 2 and 30 MHz are passed through the low-pass filter with little attenuation. Frequency components above 30 MHz, however, are sharply attenuated to reduce mixer responses and pump signal leakage. The inductors in the low-pass filter are factory-adjusted, and should not be adjusted in the field. A coaxial jumper between connectors J5302 and J5303 may be removed in order to allow testing of the two sections individually.

c. Preamplifier A1A1. The preamplifier (fig. 2–8) consists of a conventional two-stage transis-



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A1A1
   SECONDARY TRANSMITTER 6A11A1A1
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN PICOFARADS.

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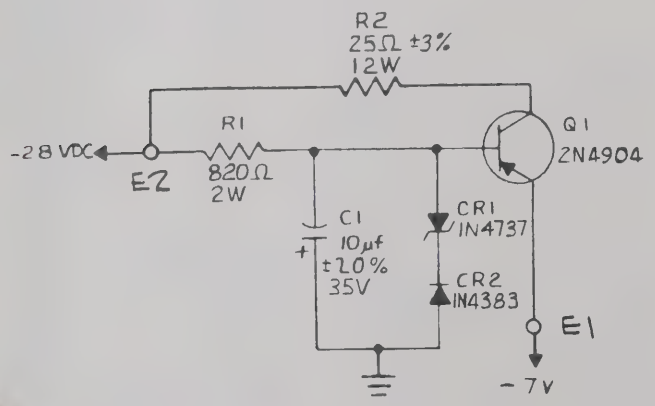
Figure 2–8. Preamplifier (A1A1), schematic diagram.

torized amplifier furnishing 10 db of gain over the frequency range of 2–30 MHz. The output of the low-pass filter is coupled to the preamplifier through connector J6601, amplified in transistors Q1 and Q2 conventionally, and the output is coupled through connector J6602 to the video amplifier (A1A3).

d. Video Amplifier A1A3. The video amplifier (A1A3) (fig. FO–15) provides a 30-db power gain with essentially flat response over the entire 2–30-MHz range of frequencies. The amplifier consists of six stages operated in Class A to provide optimum linearity. Input transistors Q5 and Q6 are low-level voltage amplifiers designed to provide sufficient signal to adequately drive transistor Q1. Amplifier stages Q1 through Q4 are operated as power amplifiers. The output of transistor Q4 is routed through connector J5203 and transmitter rear panel connector J5401 to the external LPA. In addition, the output signal is detected with diode CR1, and the resultant signal is applied to the tune leveler circuit input stage. Additional biasing furnished by the −7 Vdc voltage regulator (A1A6) serves to insure that the amplifier stages will operate in the most linear portion of their dynamic range, and thus introduce a minimum of harmonic or intermodulation distortion products. Bypass circuits are used throughout to decouple the RF signals from the +20 and −7 Vdc power circuits.

e. −7 Vdc Voltage Regulator A1A6. The −7 Vdc voltage regulator (A1A6) (fig. 2–9) drops the −28 Vdc input voltage across resistor R1 and Zener diode CR1, which is in series with temperature-compensating diode CR2 to provide a regulated −7 Vdc output at the emitter of transistor Q1 which is utilized in the video amplifier (A1A3) power stages.



NOTE:
REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
PRIMARY TRANSMITTER 6A9A1A6
SECONDARY TRANSMITTER 6A11A1A6

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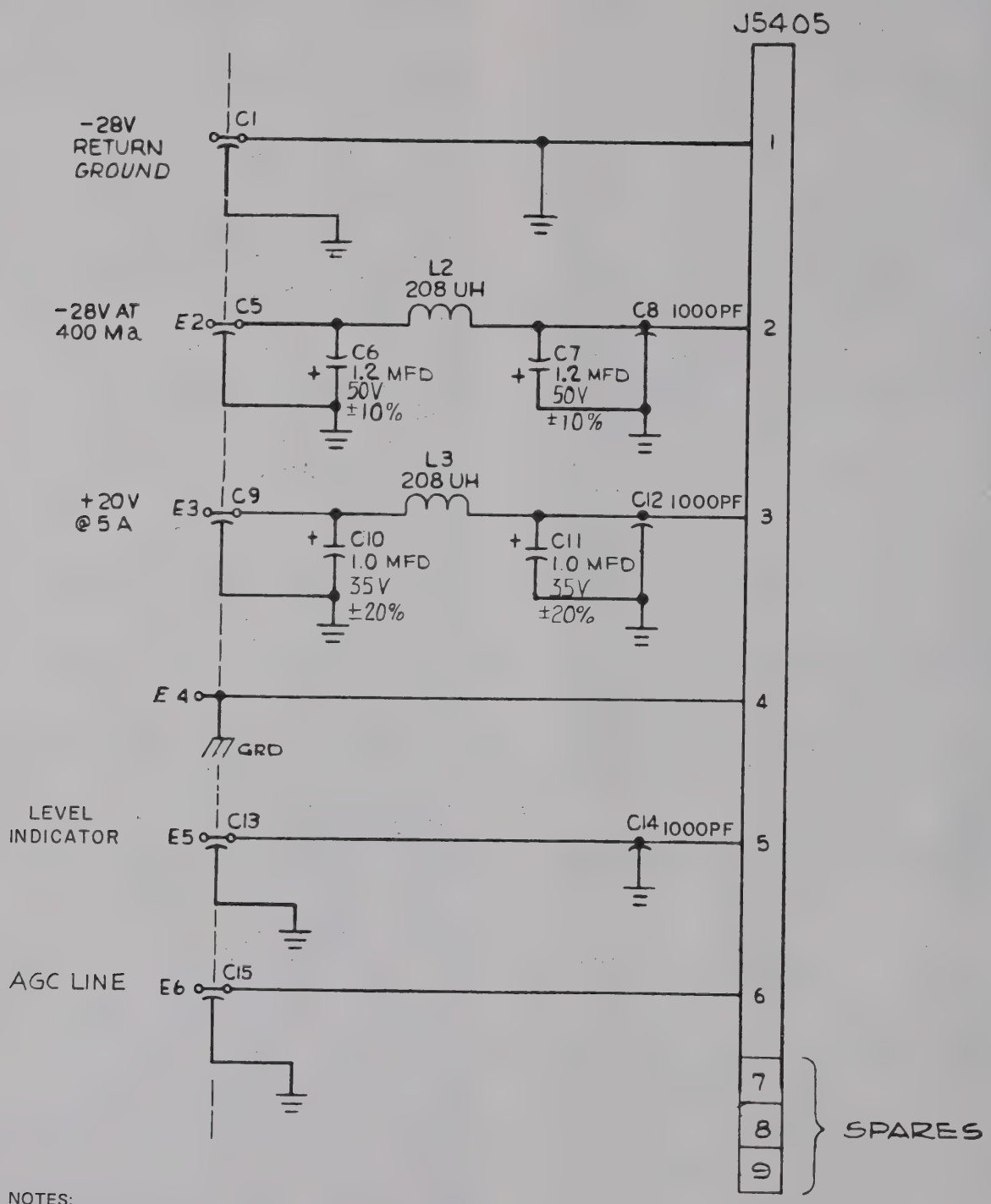
Figure 2–9. −7-volt voltage regulator (A1A6), schematic diagram.

f. Filter Box A1A4. The filter box assembly (A1A4) (fig. 2–10) provides filtering components and routing for the dc power circuits, the AGC voltage, and the carrier level indicator signal. The assembly contains RF filter components as required to obtain added decoupling of the power leads.

2–13. Frequency Select Analysis

The frequency select circuits store the digital frequency select information supplied from the frequency select panel (7A4/7A11). It then decodes the stored information to provide control voltages used to tune the frequency synthesizer (A2). The frequency select circuit is composed of six PC cards. Three of the PC cards are identical and comprise the frequency select memories (A13, A14, and A15). Two of the other three PC cards are nearly identical and comprise the code conversion matrices (A17 and A18). The sixth board is the band control (A16). The frequency select memories store digital information read in from the frequency select panel (7A4/7A11). The band control (A16) decodes the tens-of-MHz and units-of-MHz information from frequency select memory No. 1 (A13) and the hundreds-of-kHz information from code conversion matrix No. 1 (A17). The band control (A16) outputs are fed to the frequency synthesizer (A2) for pump VCO preset circuit selection and mixer inject selection, and to the 1–6 MHz VCO for band selection. The band control (A16) also supplies decoded units-of-MHz information to the frequency synthesizer (A2). The code conversion matrices decode the hundreds-of-kHz, tens-of-kHz, and units-of-kHz frequency data from the frequency select memories to produce control signals for the pump VCO variable divider in the frequency synthesizer (A2). Six 100-kHz coded outputs from code conversion matrix No. 1 (A17) are supplied to the band control PC card (A16) for further processing and application to the 1–6 MHz VCO in the frequency synthesizer (A2). The hundreds-of-Hz information from frequency select memory no. 3 (A15) is decoded by code conversion matrix no. 2 (A18) to produce control signals for the second L.O.

a. Frequency select Memory A13, A14, and



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A1A4
   SECONDARY TRANSMITTER 6A11A1A4
2. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.

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Figure 2-10. Filter box (A1A4), schematic diagram.

A15. The frequency select memory (fig. FO–16) consists of three identical PC cards (A13, A14, and A15). Each board contains 10 identical circuits; each circuit consisting of a flip-flop and a read-in gate. Signals are read into memory when a digital tune enable (DTE) signal is supplied from the frequency select panel (7A4/7A11) to the transmit gain control (A4) circuit. The resultant reset signal clears all the flip-flops in the frequency select memory to zero and allows new frequency information to read into the memories. Once the information is read in, the flip-flops do not change state again until another reset signal is applied, causing another reset. When the information is stored, changing the digital frequency information will have no effect until the next reset signal is applied.

(1) The logic reset is accomplished by a circuit located on the transmit gain control PC card A4. The DTE (ground) signal results in the development of a 40-ms pulse having the desired rise and fall time characteristics. The output is applied via pin h on the frequency select memory PC cards.

(2) The read-in process begins when a positive reset signal is supplied through pin h to the base of Q3 in all frequency select memory flip-flop circuits. Since all the circuits are identical, only the operation for circuit A will be described. The positive reset pulse causes Q3 to conduct, causing the output at pin T to go to ground, and gating off Q2. The positive reset pulse is also supplied through R1 to the base of Q1. If the pattern of signals supplied from the frequency select panel is such that a ground (+0.7V) is supplied to pin S, Q1 will conduct, discharging C1. When the positive reset pulse is removed, Q1 is gated off, disconnecting the frequency select panel signal from the flip-flop. Removing the positive pulse also permits the ground potential on C1 to appear at the base of Q3. This causes Q3 to be gated off and produces a positive output at pin T. Due to the flip-flop action, Q2 is now gated on and the flip-flop Q2–Q3 is in the one state. It will remain in this state until the next reset pulse occurs. If there is no ground at pin S from the frequency select panel (7A4/7A11) when the positive reset pulse occurs, Q1 does not conduct and C1 is allowed to charge positively through R2. As a result, when the reset pulse is removed, no ground potential is available from C1 to switch Q3. Thus it remains in the conducting state, and flip-flop Q2–Q3 stays in the zero state, causing a ground to be supplied through pin T.

(3) The digital frequency select information from the frequency select panel (7A4/7A11) is arranged in a two-out-of-five code. Hence, five flip-flops are required to store each digit of the frequency word, and at any given time two of the input lines are grounded and the other three are open-circuited. The two-out-of-five code is given in table 2–1. The 10s-of-MHz digit is an exception. Since only the numbers 0, 1, and 2 can occur in this place, this frequency digit is supplied as a two-out-of-three code. The number 0 is represented by 011, the number 1 by 110, and the number 2 by 101. The frequency select memory board associated with this digit uses circuits A, B, and C only (circuits D and E are not required). The outputs of the frequency select memories are supplied to the band control and code conversion matrices.

b. Band Control A16. The band control (fig. FO–17) processes signals which accomplish the following selections:

(1) The first digit of the variable divider-synthesizer pump division ratio (1, 2, 3, 4, 5, or 6)—J311–3, –15, and –16.

(2) Injection frequency from the harmonic generator to the hf VCO mixer (90, 85, 80, 75, 70, or 65 MHz)—J311–20, –22, –24, –27, –32, –31.

(3) Hf VCO preset (1 of 6 bands)—J311–20, –22, –24, –27, –32, –31.

(4) 3–6-MHz VCO band (A, B, or C)—J311–1 and –13. (Band A selected in the absence of signals on J311–1 and –13).

(5) 1–6-MHz VCO divider ratio (÷1, ÷2, or ÷4)—J311–6, –19, –5. The relationships between these quantities are shown in tables 2–2, 2–3, and 2–4.

(*a*) The inputs to the band control (A16) are derived from the units-of-MHz and 10's-of-MHz signals from frequency select memory No. 1 (A13) and from the 100's-of-kHz signals from code conversion matrix No. 1 (A17). These inputs are converted to the needed control voltages. These logic functions are accomplished with integrated circuit NAND gates and AND/NOR invert gates.

(*b*) The 100's-of-kHz input is already processed by code conversion matrix No. 1 (A17), and is applied as logic control data to the band control (A16). The units-of-MHz and 10's-of-MHz inputs, however, represent actual frequency values. In order to process these inputs, the band control (A16) logic converts the units-of-MHz information from two-out-of-five code to one-out-of-10. This is supplied as control infor-

Table 2-3. 3-6-MHz Oscillator Band Selection Data

Units of MHz	100's of kHz	Band A	Band B	Band C
0	0–7		x	
	8–9			x
1	0–9			x
2	0–1		x	
	2–4			x
	5–8	x		
	9		x	
3	0–3		x	
	4–9			x
4	0–7	x		
	8–9		x	
5	0–7		x	
	8–9			x
6	0–9			x
7	0–1		x	
	2–4			x
	5–8	x		
	9		x	
8	0–3		x	
	4–9			x
9	0–7	x		
	8–9		x	

Band A = 3.001–3.8 MHz = neither Q1 nor Q2 conducting.
Band B = 3.801–4.800 MHz Q1 conducting.
Band C = 4.801–6.000 MHz Q2 conducting.

mation for those circuits in the frequency synthesizer (A2) that require units-of-MHz selection. The 10's-of-MHz information is processed as a two-out-of-three code, and the 100's-of-kHz information is used in its input code form.

(*c*) An example of how the units-of-MHz information is processed follows. The two-out-of-five input code shown in the truth table on figure FO–17 indicates the voltage levels (+V or ground) existing on input pins 41, 40, 39, 38 and 34, for numbers between 0 and 9. Connected to these pins are 10 gates corresponding to the numbers 0 through 9; that is, gate G6D=0, G6A=1, through G6B=9. The code for input number 5, as shown on the truth table, is GG-VVG (or 00110), at pins 41, 40, 39, 38 and 34 respectively. (For any number, two and only two of the inputs must be 1 or high.) The gate corresponding to 5 is G17C, and both inputs to this gate are high, so they both represent 1s at pins 39 and 38. Gate G17C is the only one actuated; hence the output of this gate is low. (Since the signals applied to the other nine gates are combinations of high and low, the remaining nine gates produce high outputs.) In order to output the 5 to, *for example*, the variable divider synthesizer pump, the signal at pin J311–3 must be high. This condition exists if any input to gate G2A is low. Since the low at the G17C output is connected to G2A, the routing requirements for a 5 output to the VDSP is satisfied.

(*d*) Processing of the 10s-of-MHz information is accomplished in a similar manner. As indicated by the truth table, a 0 in the 10s-of-

Table 2-4. Organization of Frequency Synthesizing Circuits

Major section	Module, assembly, or loop	Ref des
Master clock signal generating section	Master clock oscillator	A2A9
	Master clock divider (p/o RF box No. 1 A2A5)	A2A5A1
	Filter box assembly (common to all sections of frequency synthesizing function).	A2A8
Pump signal generating scetion	Hf (pump) VCO loop:	
	Hf (pump) VCO assembly	A2A3
	Hf (pump) VCO control loop	A2A3A2
	Hf (pump) VCO preset	A2A3A1
	In-lock indicator	A2A3A3
	5-MHz amplifier assembly	A2A1
	Harmonic generator:	
	Harmonic selector	A2A2
	Buffer amplifier	A2A2A2
	Video amplifier and mixer	A2A2A3
	Logic control board	A2A2A1
	1–6-MHz VCO loop:	
	1–6 MHz VCO module	A2A7
	Variable divider synthesizer pump (p/o RF box No. 2 A2A6).	A2A6A1
	1–6-MHz phase lock loop control (p/o RF box No. 2 A2A6).	A2A6A2
L.O. signal generating section	Second L.O. RF section	A2A4
	Second L.O. variable divider (p/o RF box No. 1 A2A5)	A2A5A2

MHz position is represented by a 011 code (at pins 14, 18, and 17 respectively). A 1 in the 10s-of-MHz position is represented by 110; a 2 by 101. The configuration of NAND gates G7D, G7B, and G7A is such that G7D conducts for 2, G7B for 1, and G7A for 0. A routing for a 2 in the 10s-of-MHz position is provided via NAND gate G7D, inverting gate G18A, and one of gates G3B, G12A, G3A, G12C, and G12B. Which of the latter gates will be actuated depends upon the number selected and processed in the units-of-MHz position. Assuming a 5 in the units-of-MHz position, the gate actuated will be G12C to satisfy a requirement for a high at pin 22 (the 22–26.9-MHz output pin). The other high input at G12C is provided by gate G1B, one of whose inputs (G17C) represents the 5 output in the units-of-MHz position, and is therefore low.

(*e*) The units-of-MHz and 10s-of-MHz information is processed to select a particular pump VCO preset circuit (A2A3A1), mixer injection frequency, 1–6-MHz VCO band, and division ratio. For example, if the units-of-MHz input is 2, the signal levels appearing at pins 41 and 39 of connector J311 will be high (logic 1) and those appearing at pins 40, 38, and 34 will be low (logic 0). This combination of signals produces the logic word 10100 (following the pin sequence listed in the truth table). If, at the same time, the 10s-of-MHz digit is a 0, the signal at pin 14 is low and the signals at pins 17 and 18 are high (logic word 011). After processing through the band control (A16) circuits, these signals produce a high at pins 19 or 5 (depending upon 100 kHz selection) 16, and 31 of connector J311. The signal on pin 19 or 5 is fed to the 1–6 MHz VCO (A2A7) in the frequency syntehesizer to select Band II ÷2 or band I÷4. The signal on pin 16 goes to the VDSP. The signal on pin 31 goes to the pump VCO module in the frequency synthesizer (A2) causing the 90-MHz injection frequency and the proper pump VCO preset to be selected. Other VDSP division ratios, mixer injection frequencies, hf VCO presets and 1–6-MHz VCO bands are selected in a similar manner for the other combinations of 10s-of-MHz and units-of-MHz digits.

(*f*) The units-of-MHz information is used to control the most significant digit in the division ratio of the variable divider synthesizer pump (A2A6A1). The VDSP is a divide-by-6000 counter, which can be made to divide in any ratio from 1001 to 6000. To accomplish the variable division, a number which is the difference between 6000 and the desired division ratio is preset into the counter before the counting process is started (table 2–2). If the operator-selected frequency setting is 2.000 MHz, the division ratio of the VDSP will be 1001, and the required preset will therefore be 4999 (6000–1001). For every 1 kHz that the frequency setting is increased from 2 MHz, the division ratio also increases by 1, and the required preset therefore decreases by 1. This continues for a 5-MHz segment which ends with the frequency setting 6.999 MHz. In this case, the division ratio is 6000 and the required preset is 0000. For the 5-MHz increment starting with 7.000 MHz and ending at 11.999 MHz, a different harmonic generator injection frequency (85 MHz) is used in the pump phase-locked loop (A2A6A2) and the division ratio starts another cycle from 1001 to 6000. For each subsequent 5-MHz increment, the division ratio cycle is repeated up to the frequency of 26.999 MHz. The next cycle (from 27.000 to 29.999 MHz) is only a 3-MHz increment; consequently, on this last cycle, the division ratio goes from 1001 to 4000.

(*g*) The number appearing in the most significant place in the preset count also changes with the change of the number appearing in the units-of-MHz place. In each cycle, whenever a 2 or 7 occurs in the units-of-MHz, a 4 is required in the most significant place of the preset count (table 2–2). Similarly, a 3 or 8 requires a 3; a 4 or 9 requires a 2; a 5 or 0 requires a 1; and a 6 or 1 requires a 0 in the most significant preset count digit. The equivalent binary word for the first digit of the preset is contained in the first three digits of the complete binary preset word. The 0 indicates a low and the 1 indicates a high applied through pins 3, 15, and 16 of connector J311 to the VDSP. The voltages at these pins are derived from outputs of gates G2A, G2B, and G16C, with G16C being the most significant digit. The outputs of these gates are derived from the pattern of voltages supplied to gates G6B, G6D, G16B, G16D, and G17A through G17D. Thus, if the units-of-MHz digit of the tuneup frequency is either a 2 or a 7, voltage fed to gate G16C results in a positive voltage at pin 16, and the outputs of G2A and G2B remain low. This corresponds to the binary character 100 which is a decimal 4. If the unit digit is a 1 or 6, no positive inputs are supplied to gates G2A, G2B, or G16C, resulting in the character 000, or a decimal 0. The other characters in the first column of the equivalent binary word portion of the table are generated in a similar manner. The binary characters for the second and third numbers are

derived from outputs of code conversion matrix No. 1 (A17). The characters for the fourth number are derived from code conversion matrix No. 2.

(*h*) The 100s-of-kHz and units-of-MHz information is used to select the 1–6-MHz VCO band and divider that will provide the desired 1–6-MHz VCO output frequency to the pump VCO and the VDSP. The 100s-of-kHz signals are applied from code conversion matrix No. 1 (A17) to the band control (A16) via pins 7, 8, 9, 10, 11, and 12 of connector J311. The pattern of voltages for the 100s-of-kHz settings is shown on the truth table of the schematic diagram (fig. FO–17). The units-of-MHz information is applied from frequency select memory No. 1 (A13) in a two-out-of-five code to pins 34, 38, 39, 40, and 41 of J311. Initial processing of the units-of-MHz information through NAND gates produces a one-out-of-10 code. This code is then combined with the 100s-of-kHz code to select the desired band and division output of the 1–6 MHz VCO. *For example,* if the tuneup frequency is 5.9991 MHz, the units-of-MHz digit is 5 and the 100s-of-kHz digit is 9. For this combination, the logic must select lf VCO (low frequency VCO) band C (4.8–6.0 MHz) with a Band III +1 ratio for the output of the 1–6 MHz VCO (tables 2–2 and 2–3). Thus a 5 (binary word 01100) appears at pins 34, 38, 39, 40, and 41 of connector J311. A 9 (binary word 110101) appears at pins 7, 9, 11, 8, 10, and 12 of J311. These combinations of high and low signals cause outputs at pins 13 and 6 of connector J311 which select the desired band and divisor of the 1–6 MHz VCO. The 100s-of-kHz binary code 110101 places a positive voltage (high) on pins 7, 9, 8, and 12 of J311 and grounds (low) on pins 11 and 10. The high signals on pins 7, 9, 8, and 12 are fed to AND/NOR gate G14 for combining with signals of the one-out-of-10 information and the low signal from pin 7 of connector J311. Because a 5 is selected for the units-of-MHz digit, the G17C output is low and all other outputs of the one-out-of-ten gates (G6A, B, C, and D, and G17A, B, and D) are high. Observe the effects of this set of conditions on gates G15 and G5B which select lf VCO band C through Q2 and pin 13 of J311. The G6C output presents a high to G5B, as does the G6A output. Thus neither of these two signals can produce the high output of G5B which is necessary to gate on Q2 (whose conduction operates the relay in the lf VCO to select the 4.8–6.0-MHz band). Hence the G15 output must be low if band C is to be selected. The G15 output is supplied from a NOR gate, and if the output is to be low, one of its inputs must be high. The input at pin 6 of G15 is a low from J311–11 and pin 5 receives a low from G9C; hence these inputs cannot produce the required low output from G15. The pin 2 output to G15 is a high from J311–12 but since the input to pin 3 is a low from G8C, these inputs cannot produce the required low output from G15. The pin 13 input to G15 is a high from J311–7 and it combines with the high on pin 1 from G8A to produce a high input to the NOR gate, which in turn provides the low output of G15. The low on pin 5 of G5B causes a high at pin 6 which gates on Q2. The inputs to gate G14 produce a high output which prevents Q1 from being gated on and thus insures that bands B and C are not selected simultaneously. The G14 output can be low only if highs are supplied simultaneously to both inputs of any one of the input pairs. Under the stated input conditions, pin 13 of G14 receives a high from J311–8 but pin 1 receives a low from G9C; pin 2 of G14 has a low from J311–10 and pin 3 has a low from G8C; pin 9 has a high from J311–7 but pin 10 has a low from G8D; and pin 5 has a low from G11D (an inversion of the low at J311–7) and pin 6 a high from G8A. None of these sets of inputs will provide the low output from G15 which is required to gate-on and select band B.

(*i*) Selection of the operating band and divider ratio of the lf VCO depends upon the tuneup frequency of the transmitter, which establishes the output frequency desired for the 1–6 MHz VCO. As discussed previously, band B (3.8 to 4.8 MHz) is selected when Q1 is switched on, resulting in a relay actuation signal at pin 1 of J311. Band C (4.8 to 6.0 MHz) is selected when Q2 is switched on, resulting in a relay actuation signal at pin 13. In the absence of a signal at both pins 1 and 13, the VCO operates in band A (3.0 to 3.8 MHz). Actuating the appropriate divisor circuit (+4, +, or +1) in combination with the desired band permits selection of any frequency in the 1–6-MHz range. The relationship between the bands and the units-of-MHz and the 100-kHz digits of the tuneup frequency is shown in table 2–3.

c. Code Conversion Matrices A17 and A18. The frequency select section contains two code conversion matrix PC cards that provide code conversion from the two-out-of-five code to 9s complement BCD code for 100s-of-kHz, 10s-of-kHz, and units-of-kHz digits and to the X-out-

of-five code for the 100s-of-Hz digits. The conversion for 100s-of-kHz and 10s-of-kHz is accomplished on code conversion matrix No. 1 (A17) and the units-of-kHz and 100s-of-Hz are converted on code conversion matrix No. 2 (A18). Code conversion matrix No. 1 (A17) also provides six logic signals that are applied to the band control A16 PC card. Code conversion is accomplished by processing the input signals through integrated circuit NAND gates, as discussed below.

(1) Code conversion matrix No. 1 (A17) consists of two sections; circuit A1 and circuit A2, for processing the 100s-of-kHz and 10s-of-kHz codes respectively (fig. FO–18). Both circuits receive data inputs in 2-out-of-5 code from the frequency select memory No. 2 (A14) PC card. Circuit A1 outputs are applied to the variable divider synthesizer pump (A2A6A1) on pins N, P, R, and S, and to the band control (A16) on pins C, D, f, A, j, and Z. An example of how code conversion is accomplished follows. As shown in the truth table of figure FO–18, the number 5, for example, is represented in 2-out-of-5 code by the word 00110 on inputs pin F, H, J, K, and L. Applying the 5 code results in a low at the output of G2B and highs at the other NAND gates in the first bank of gates. When processed by the second band of NAND gates, the code at the VDSP input from pins NPRS is 0100 corresponding to the number 5 in 9s complementary BCD. The word appearing at card A17 output pins C, D, f, A, j, and Z is 010001 corresponding to the code for 5, which is routed to the band control (A16).

(2) Code conversion matrix No. 2 (A18) also consists of two sections; circuits A1 and A2 respectively. The data inputs are received from frequency select memory No. 3 (A15). After conversion in the manner described above, the output codes are routed to the VDSP (units of kHz) and the variable divider 2nd L.O. (units of Hz). Code conversion matrix No. 2 (A18) is illustrated in figure FO–19.

2–14. Frequency Synthesizer A2 Analysis (fig. FO–20)

The frequency synthesizer (A2) consists of various modules and assemblies which are organized functionally into three basic sections: a master clock signal generating section, an hf pump signal generating section, and an L.O. signal generating section. These sections are contained in a completely inclosed RF-tight package. Since the circuit locations are independent of electrical functions, a tabulation of the various assemblies and modules in relation to the major sections is shown in table 2–4. Interconnections of the frequency synthesizer (A2) subassemblies and modules are shown in figure FO–47. As indicated in table 2–4, the master clock signal generating section contains the 5-MHz master clock (A2A9) and master clock divider (A2A5A1) which provide the fundamental reference and other reference frequencies used within the function and the 100-kHz reference used in the modulation and control functions. The L.O. signal generating section consists of the second L.O. variable divider (A2A5A2) and the second L.O. RF section (A2A4). These circuits develop the second L.O. signal for the RF translator (A1). The pump signal generating section is composed of the hf (pump) VCO (A2A3) pump VCO error detection circuits, 1–6 MHz VCO (A2A7), 1–6-MHz VCO variable divider (A2A6A1), 1–6-MHz VCO phase detector (A2A6A2), harmonic generator and mixer (A2A2), and in-lock indicator circuit (A2A3A3). The frequency synthesizing function provides digital tuning in 100-Hz steps with a stability of 1×10^{-8} per day. In the pump signal generating section, two phase-lock loops combine to provide the first L.O. frequency in 1-kHz steps from 88.999 to 61 MHz for the first mixer. A third phase-lock loop (L.O. signal generating section) provides the second L.O. frequency in 100-Hz steps from 90.8990 to 90.8999 MHz. All three loops are referenced to the 5-MHz master clock. Additional RF shielding of some of the synthesizer assemblies is furnished by enclosing them in RF-tight housings within the synthesizer inclosure. Thus, RF box No. 1 (A2A5) houses the second L.O. variable divider (A2A5A2) and the master clock divider (A2A5A1). Additionally, it houses the components of a low-pass filter used with the 100-kHz reference signal which is supplied to the modulation and control circuits. RF box No. 2 (A2A6) contains the circuit boards for the variable divider synthesizer pump (VDSP) (A2A6A1) and the 1–6-MHz phase-lock loop control (A2A6A2).

a. Master Clock Signal Generating Section. The master clock signal generating section contains the 5-MHz master clock (A2A9) and the master clock divider (A2A5A1). This section provides fundamental reference frequencies utilized throughout the frequency synthesizer (A2) as well as the 100-kHz reference frequency applied to the modulator and control circuits of the transmitter.

(1) *5-MHz Master Clock A2A9.* The 5-MHz master clock (A2A9) is a highly stabilized, crystal-controlled oscillator with a frequency stability of $\pm 1 \times 10^{-8}$ after a 1-hour warmup period. The clock output is the basic 5-MHz signal which is routed to the master clock divider (A2-A5A1), the harmonic generator, and the second L.O. RF section (A2A4).

(2) *Master Clock Divider A2A5A1.* The master clock divider (A2A5A1) (figs. FO–21 and FO–22) is included in RF box No. 1 (A2A5) and receives the 5-MHz signal from the master clock. The divider then divides the basic 5 MHz to provide 1-MHz, 100-kHz, 10-KHz, 1-kHz, and a 100-Hz ramp output. Frequency division is accomplished in five discrete, series-connected sections. The first section (a divide-by-5 circuit) is followed by four divide-by-10 sections. The 5-MHz signal from the master clock is applied to a squaring circuit composed of tunnel diode CR1 and transistors Q1, Q2, and Q3. Tunnel diode CR1 acts as a snap-action diode to clip the peaks of the incoming 5-MHz signal. Transistor Q3 amplifies the squared pulse and couples it to the complementary transistor pair Q1–Q2. These transistors clamp the positive and negative peaks to a level of +6 volts and 0 volt respectively, and serve as a driver for the following flip-flops. Each section of the count-down chain is a synchronous counter. Thus, the clock pulse driving the counter is applied simultaneously to each stage within the counter, and steering inputs assure that the proper stages change state. Integrated circuit flip-flops are utilized throughout the countdown chain. The truth table for each IC stage is shown on figure FO–22. The first section of the countdown chain is a divide-by-five counter. It consists of three IC flip-flops (FF1, FF2, and FF3), and a NAND gate (G1–C) which all work in conjunction to produce a single output from FF1 pin 12 for every five input pulses from transistor pair Q1–Q2. The truth table for this counter is shown on figure FO–22. The 1-MHz output from the divide-by-five counter chain is applied to the second L.O. RF section (A2A4 fig. FO–38) and to the following divide-by-ten circuits. All sections of the countdown chain which comprise the divide-by-ten counters are identical. Each one consists of five IC flip-flops and a NAND gate. A truth table for the divide-by-ten counters is shown on figure FO–22. A buffer amplifier transistor (Q11) applied the 100-kHz output of the first divide-by-ten counter chain through a low-pass filter (fig. FO–38) located in RF box No. 1 (A2A5), and then out to the control circuits and the modulation circuits where it is used as one of the injection frequencies. The output of the third divide-by-ten divider chain is a 1-kHz signal fed to a ramp generator in the 1–6-MHz phase-lock loop circuit (A2A6-A2). The output of the fourth divide-by-ten divider chain is a 100-Hz signal fed to another ramp generator consisting of transistors Q8, Q9, and Q10, along with diodes CR5, CR6, and CR7. In this circuit, transistor Q8 is a transistor switch, transistor Q9 serves as a constant current source, and transistor Q10 is configured as an emitter follower. The bias voltage on the transistors is regulated by diode CR7 and resistor R31. The input signal, as a square wave, is applied to the base of transistor Q8 through diodes CR5 and CR6. These diodes serve to provide isolation and are switching devices. The input square wave causes transistor Q8 to be triggered into saturation, which causes the junction of resistor R34 and the base of transistor Q10 to assume a level just above ground potential. Since transistor Q10 is an emitter follower, the emitter is likewise at approximately 0 Vdc. When the input square wave on the base of transistor Q8 drops, the conduction of transistor Q8 stops, and allows the state of charge on capacitor C4 to increase at a linear rate, approaching the +17 Vdc level on the emitter of transistor Q9. The charge path for capacitor C4 is through resistor R34 and the collector emitter path through transistor Q9. Following conventional emitter follower conventions, the signal at the emitter of transistor Q10 follows the signal on the base, and the ramp signal appears on the emitter of transistor Q10. The signal is coupled through pin 15 of connector J3101 to the second L.O. variable divider (A2A5-A2) PC card.

b. Hf (Pump) Signal Generating Section. The hf (pump) signal generating section (figs. FO–23 and FO–49) utilizes two control loops in order to provide the pump signal to the RF translator (A1). These loops are the hf VCO control (A2A3A2) and the 1–6 MHz VCO (A2-A6A2). The pump signal developed by hf VCO (A2A3) is a range of frequencies between 61.000 and 88.999 MHz. The hf VCO loop consists of the hf (pump) VCO (A2A3), buffer amplifier (A2A2A2), video amplifier and mixer (A2A2A3), harmonic selector (A2A2), phase detector (A2A6A2), preset (A2A3A1), in-lock indicator (A2A3A3), and various impedance matching and isolation circuits. The band select signals from the frequency select circuits deter-

mine the desired frequency band (within 61–89-MHz range) of the pump VCO. The loop circuits provide the coarse and fine frequency controls to ensure that the VCO is held precisely on frequency in phase-lock at the selected frequency. This is accomplished by comparing (in the phase detector circuitry) a down-converted sample of the pump signal with a stable reference signal derived from the other loop. The comparison is actually made in the range of 1 to 6 MHz and is based on the reference signal derived from the 1–6-MHz VCO output. Use of the 1–6-MHz VCO signal as a reference for the pump VCO loop greatly simplifies the logic circuitry required for precise control of the 280,000 output frequencies and offers other advantages such as signal purity, low frequency jitter, and low noise levels. The 1–6-MHz VCO loop consists of the 1–6 MHz VCO (A2A7), the 1–6-MHz VCO phase detector and frequency discriminator (A2A6A2) and the variable divider synthesizer pump (VDSP) (A2A6A1). The frequency select signals from the frequency select circuits determine the desired frequency (within the 1–6-MHz range) of the 1–6 MHz VCO. The loop circuits provide the coarse and fine frequency controls to ensure that the VCO is held precisely on frequency and in phase-lock at the frequency selected by the frequency select circuits. This is accomplished by comparing a divided-down sample of the 1–6 MHz VCO with a stable 1-kHz reference derived from the master clock divider (A2A5A1). The comparison is accomplished in the phase detector and in the frequency discriminator circuits. The relationships between the transmitter tuneup frequency, control loop frequencies, bands, ranges, and divider ratios are shown in table 2–5. Columns 1 and 2 show the relationship between the pump VCO preset bands and the selected tuneup frequency. Column 3 shows the injection frequencies of the harmonic generator for the pump preset bands and frequency ranges (col. 4). The divisors used by the VDSP to count down the 1–6-MHz VCO frequency to 1 kHz are listed in column 5. The relationship between the output frequencies of the 1–6 MHz VCO and the VDSP counting range (col. 5 and 6) are shown only for the case of hf VCO preset band No. 1. The comparable relationships for the five remaining preset bands may be derived by following the same sequence. The entries in column 7 (lf VCO band) refer to the frequency ranges of the 3–6-MHz VCO circuit (from which the 1–6-MHz VCO output is obtained). The entries in columns 8 and 9 indicate how the frequencies noted in column 6 are derived from the 3–6-MHz oscillator. The pump VCO provides stable signals in the range of 88.999–61.000 MHz in 1000-Hz steps. These signals are applied to the RF translator (A1) where they are heterodyned with the 91-MHz IF to yield the transmitter output frequencies in the 2.0–29.999-MHz range. A sample of the pump VCO frequency is also applied to a mixer circuit in the harmonic generator and mixer circuits for processing in the frequency and phase-locked loops. These loops are stabilized against a reference signal from the 1–6 MHz VCO. When the tuning process is initiated by the frequency select circuits, an appropriate frequency band within the operating range of the hf (pump) VCO is also selected from a preset circuit (fig. FO–23). Six frequency bands are provided by the preset circuit to enable the pump VCO to cover the 88.999–61-MHz spectrum. The output of the VCO is applied to the RF translator (A1) and also to the mixer stage in the harmonic generator where the VCO signal is mixed with a high frequency injection signal developed within the harmonic selector (A2A2). The injection signal is in the 65–90-MHz range, and is derived as a harmonic of the 5-MHz input from the master clock (A2A9). In the 5-MHz amplifier (A2A1), the signal is changed to a pulsed signal rich in harmonics of 5 MHz. The particular harmonic frequency generated is determined by the mixer injection select logic (six lines) from the frequency select circuits. The selected harmonic, which is separated into frequency components by the harmonic selector, has a frequency of 65, 70, 75, 80, 85, or 90 MHz. The selected frequency is mixed with the pump signal to yield a difference video in the 1–6-MHz range when the pump is at the proper frequency for tuning the transmitter to the desired frequency. The resultant signal is applied to the pump frequency and phase-correction loops, where it is compared and locked to the 1–6-MHz reference signal. Before the loop can be brought into phase lock, the difference video and the 1–6-MHz reference must be close in frequency. A frequency discriminator brings the loop within the acquisition range of the phase-lock circuit. To accomplish this, the frequency discriminator compares the difference video output of the mixer with the 1–6-MHz reference signal.

NOTE

The actual reference frequency varies from 1.001 MHz to 6.000 MHz in 1-kHz steps. In subsequent discussions, the sig-

Table 2-5. Control Loop Frequencies, Bands, Ranges and Divider Ratios

Tuneup frequency range (MHz)	HF (Pump) VCO preset band No.	Harmonic generator injection (MHz)	HF (Pump) VCO frequency range (MHz)	VDSP Counting range		1-6-MHz VCO output frequency (MHz)	LF VCO band*	LF VCO frequency (MHz)	LF VCO divider ratio
2.000	1	90	88.999-88.000	1001-2000		1.001-1.200	B	4.004-4.800	4
through	1	90	87.999-86.000	2001-4001		1.201-1.500	C	4.804-6.000	4
6.999	1	90	85.999-84.000	4001-6000		1.501-1.900	A	3.002-3.800	2
7.000 through	2	85	83.999-81.000	1001-4000		1.901-2.000	B	3.802-4.000	2
11.999	2	85	80.999-79.000	4001-6000	**	2.001-2.400	B	4.002-4.800	2
12.000 through	3	80	78.999-76.000	1001-4000		2.401-3.000	C	4.802-6.000	2
16.999	3	80	75.999-74.000	4001-6000	**	3.001-3.800	A	3.001-3.800	1
17.000 through	4	75	73.999-71.000	1001-4000		3.801-4.000	B	3.801-4.000	1
21.999	4	75	70.999-69.000	4001-6000	**	4.001-4.800	B	4.001-4.800	1
22.000 through	5	70	68.999-66.000	1001-4000		4.801-6.000	C	4.801-6.000	1
26.999	5	70	65.999-64.000	4001-6000	**				
27.000 through	6	65	63.999-61.000	1001-4000	**				
29.999									

*The LF VCO bands are as follows:
A-3.0 to 3.8 MHz
B-3.801 to 4.8 MHz.
C-4.801 to 6.0 MHz.

**The data associated with the 1-6-MHz VCO output and the LF VCO ranges repeats for every 5-MHz change in exciter tuning. Complete data is shown only as it relates to the first Preset Band (Band 1) of HF VCO (84.000 to 88.999 MHz).

nal will be referred to by its nominal 1–6-MHz range.

The output of the discriminator is an error voltage with polarity and amplitude corresponding to the frequency deviation. The error voltage is applied to a summing network along with a portion of the dc error signal from the phase detector in the phase-correction loop. The composite error signal is amplified in the frequency loop amplifier and applied, with the pump preset voltage as a dc level derived from one of six gating circuits. The gates correspond to the six bands into which the 88.999–61-MHz frequency spectrum of the hf VCO is divided. Each band represents a particular operating range of the pump VCO. The appropriate band is selected by the digital inputs from the frequency select circuits. The phase correction loop of the pump VCO uses a phase detector to compare the phase of the difference video with that of the 1–6-MHz VCO reference signal. The phase detector output is applied to the phase loop amplifier and to the summing network as previously stated. The amplifier output is the fine-control voltage for the pump VCO. When the loop is not in phase-lock, the amplifier triggers a ramp generator which causes the VCO to sweep through its range to insure acquisition. The amplifier also provides a signal to the in-lock indicator circuit when the loop is not in lock.

(1) *Hf (pump) VCO loop.* The hf (pump) VCO loop consists of hf (pump) VCO (A2A3) (fig. FO–24), hf (pump) VCO control loop (A2-A3A2) (fig. FO–25), hf (pump) VCO preset (A2A3A1) (fig. FO–26), and in-lock indicator (A2A3A3) (fig. FO–27). In addition, a 5-MHz amplifier (A2A1) (fig. FO–28) and harmonic generator provide signal inputs to the hf (pump) VCO loop.

(*a*) *Hf (pump) VCO A2A3* (fig. FO–24). The hf (pump) VCO circuit (p/o A2A3) consists essentially of an oscillator driver (Q1) and an LC-tuned oscillator (Q2). The frequency of the oscillator is determined by the inductance of inductor L7 and the capacitance of varactor diode CR1. Fine and coarse error voltages are applied through diode CR1 and inductor L7 respectively. The fine control voltage, obtained from the phase loop amplifier (Q7 of pump VCO control loop), appears at terminal E1. Variations in this voltage cause changes in the effective capacity of CR1, which is in parallel with capacitors C8, C9, and C11 of the oscillator tank circuit. The coarse control voltage obtained from the pump VCO preset circuit is applied through capacitor C3, resistor R2, and buffer amplifier Q3 to drive transistor Q1. Variations in the conductance of transistor Q1 cause variations in the current through, and hence the inductance of, inductor L7. The pump VCO outputs (88.999–61 MHz) are routed through connector J5804 to the harmonic generator and J5805 to the RF translator (A1). The J5806 output is not used in the transmitter. A temperature control stabilizes the VCO circuit against drift due to temperature variations. The loop includes inductor L7, transistors Q4 and Q5, heating element L6, and temperature-compensating resistor RT1. The heating element, which is in the transistor Q5 collector circuit, incloses the L7 assembly and keeps it at an approximately even temperature to prevent inductance variations and resultant VCO drift. Variations in transistor Q5 conductance affect the current through heating element L6, which determines the temperature in the L7 assembly. Resistor RT1, in the transistor Q4 base circuit, acts as a variable resistance to control the bias and hence the conductance of Q4. Transistor Q4 in turn controls the conductance of transistor Q5. In summary, if the temperature in the L7 assembly tends to change, the resistance of RT1 linearly increases or decreases, as the loop requires, to cause the heating element to produce the effect required to correct for the temperature change.

(*b*) *Hf (pump) VCO control loop A2-A3A2.* The hf (pump) VCO control loop (A2A3-A2) (figs. FO–25 and FO–25A) provides coarse error signals for frequency-lock control, and fine error signals for phase-lock control. The frequency-loop control output is applied to terminal E49 and the phase-loop control to E41.

NOTE

The control loop assembly (A2A3A2) PC board is supplied in two versions and designated as assembly Nos. 233–00–274 and 233–00–640. The two are electrically equivalent but the latter has fewer components and uses integrated circuits rather than discrete components for certain functions. The 233–00–274 version is shown on figure FO–25(1). The 233–00–640 version is shown on figure FO–25①. The 233–00–640 version is shown on figure FO–25②.

1. Control loop A2A3A2 (fig. FO–25, sheet 1.) The frequency control loop employs a frequency discriminator which is composed of transistors Q10 and Q11 and associated cir-

cuitry. The discriminator compares the difference video frequency (introduced at terminal E48) with the 1–6-MHz reference (terminal E47) to produce a dc-control voltage. Transistors Q10 and Q11 produce pulses which are equal in amplitude but opposite in polarity. The Q10 output pulse rate is determined by the difference video signal frequency which is applied through amplifiers Q2, Q3, and Q4 and pin 4 of transformer T2. The Q11 output pulse rate is determined by the 1–6-MHz reference oscillator frequency which it receives from transistor Q1. The outputs are differentiated, summed, and applied to capacitor C18. If the difference video frequency is less than the reference (an out-of-lock condition), capacitor C18 receives a smaller number of negative pulses through diode CR8 than positive pulses through diode CR9, and a net positive charge accumulates on the capacitor. This positive voltage applied through differential amplifier transistor Q12 causes the loop to generate a coarse error signal which increases the hf VCO frequency. In a similar manner, a difference video frequency greater than the reference results in a negative charge on capacitor C18, which causes the hf VCO to decrease frequency. At or near lock, the two frequencies approach equality and the voltage on capacitor C18 is approximately zero. The transistor Q12 output is routed through amplifier transistor Q14, emitter-follower transistor Q15, and terminals E49 and E26 on the coarse error/coarse control afc bus on the preset assembly (A2A3A1) (fig. FO–26). The output of Q14 is also applied via diodes CR14 and CR13 to the hf VCO (A2A3) (fig. FO–24). The signal appearing at terminal E46 is a pulse reset signal from the in-lock indicator circuit (A2A3A3) (fig. FO–27). This pulse ensures that the pump VCO always approaches the required pump frequency from the low frequency limit, to minimize the effects of hysteresis in the Vari–L inductor used to preset the VCO. The reset signal is generated whenever the transmitter tuning process is initiated, or if the pump VCO loop loses phase- or frequency-lock due to a transient. The reset signal causes transistor Q16 to saturate and thereby reduce the Vari–L inductor L7 current at the pump VCO to zero. Therefore, the pump VCO tuning (or retuning) process always starts from the low frequency end of the VCO tuning range (approximately 50 MHz). The reset signal is routed via terminal E50 to capacitor C3 in the pump VCO circuit (fig. FO–24), and terminal E28 on the coarse error/coarse control bus of the preset A2A3A1 PC card. The reset signal is augmented by the voltage obtained from the transistor Q14 output, as mentioned above. This added voltage effectively shortens the time constant of the R64–R61–C1 network on the preset PC card, and thereby assures that the retuning process at the high end of the pump VCO range (band 6) always starts at the lowest frequency within the band. In the phase correction loop, the reference frequency from the 1–6 MHz VCO is applied through buffer amplifier Q1 and transformer T1 to a diode bridge phase detector consisting of diodes CR1 through CR4 (fig. FO–25①). The difference video signal appearing at terminal E48 is amplified by transistors Q2, Q3, and Q4, and is also applied (through transformer T2) to the diode bridge. The detector output at terminal 5 of T2 is a dc voltage proportional to phase error. RF components of the signal are removed by the C8, C9, and R20 network. Second harmonic components due to heterodyning of 1-MHz signals appearing at terminals E47 and E48 are eliminated by inductor L1 and capacitor C25, which form a 2-MHz trap circuit. If the loop is locked, the voltage at T2–5 is either a steady level or is varied slightly as needed to maintain phase lock. These variations appear at the Q5 base of differential amplifier Q5–Q6. The resultant varying output at the Q5 collector is applied via emitter follower Q7 and terminal E41 to the hf VCO varicap CR1 (fig. FO–24) as the fine control (phase) voltage. The dc signal appearing at the output of transistor Q7 is also applied to a ramp-generator circuit consisting of amplifier Q8, unijunction transistor Q9, and associated components. The ramp generator is quiescent as long as the varying voltage at the transistor Q8 input is below a frequency of a few Hz, since high-pass circuit R32–C13 does not pass slowly varying signals. If the loop is not locked, the signal at transistor Q5 is an ac voltage having large frequency variations. The frequency is proportional to the frequency difference between the 1–6-MHz reference signal and the difference video signal. The resulting differential voltage, which is applied through transistor Q7 to the ramp generator, is then sufficient to exceed the transistor Q9 threshold. The slope of the ramp is determined by R38, C23, and associated components in the transistor Q9 circuit. The ramp voltage at capacitor C23 is fed to the reference base of differential amplifier Q12 to provide a sweep signal at the output. This signal sweeps the pump VCO signal through the loop acquisition range to ensure phase-lock after frequency-lock has been accomplished. The dc balance of transistor Q12 is set by potentiometer R57. Since the bandwidth or error correction

range of the phase loop is small compared to that of the frequency loop, a stabilizing circuit is incorporated to coordinate the two. This circuit, an rc network composed of R25, C19, and R28, connects the phase error channel at transistor Q5, with the frequency error channel at transistor Q12. If the phase-loop is excessively unbalanced during tuning or transients, the network couples part of the large phase-error correction voltage to the frequency channel differential amplifier. This voltage actuates the frequency correction circuits for quicker stabilization of the correction loops. Conversely, during frequency correction, a portion of the relatively large error voltage developed by the frequency discriminator is applied to the phase loop. The sense of the voltage is such as to drive the phase-loop circuitry in the proper direction to null out the error once it is within the acquisition range of the phase error correction loop.

2. Control loop A2A3A2 (fig. FO–25②). In the 233–00–640 version of the hf (pump) VCO control loop (A2A3A2) (fig. FO–25②) the frequency discriminator is composed of transistors Q6 and Q7 and associated circuitry. It compares the difference video frequency (introduced at terminal E48) with the 1–6-MHz reference (terminal E47) to produce a dc-control voltage. Transistors Q6 and Q7 produce pulses which are equal in amplitude but opposite in polarity. The Q6 transistor output pulse rate is determined by the difference video signal frequency which it receives through amplifier transistor Q2. The Q7 transistor output pulse rate is determined by the 1–6-MHz reference oscillator frequency which it receives from transistor Q1. The outputs are differentiated, summed, and applied to capacitor C26. If the difference video frequency is less than the reference (an out-of-lock condition), capacitor C26 receives a smaller number of negative pulses through diode CR8 than positive pulses through diode CR11, and a net positive charge accumulates on the capacitor. This positive voltage, applied through differential amplifier AR2, causes the loop to generate a coarse-error signal which increases the hf VCO frequency. In a similar manner, a difference video frequency greater than the reference results in a negative charge on capacitor C26, which causes the hf VCO to decrease frequency. At or near lock, the two frequencies approach equality and the voltage on capacitor C26 is approximately zero. The AR2 amplifier output is routed through terminal E49 to E26 in the coarse error/coarse control AFC bias on the preset A2A3A1 PC card (fig. FO–26). The output is also applied via transistor Q9, resistor R55, diode CR13, and transistor Q8 to the hf VCO (A2A3), as described below. The signal appearing at terminal E46 is a pulse reset signal from the in-lock indicator circuit A2A3-A3 (fig. FO–27). This pulse ensures that the pump VCO always approaches the required pump frequency from the low frequency limit to minimize the effects of hysteresis in the Vari–L inductor L7 used to preset the VCO (fig. FO–24). The reset signal is generated whenever the transmitter tuning process is initiated, or if the pump VCO loop loses phase- or frequency-lock due to a transient. The reset signal causes transistor Q8 to saturate and thereby reduce the Vari–L inductor control current at the pump VCO to zero. Therefore, the pump VCO tuning (or retuning) process always starts from the low frequency end of the VCO tuning range (approximately 50 MHz). The reset signal is routed via terminal E50 to capacitor C3 in the pump VCO circuit, and terminal E28 on the coarse error/coarse control bus of the preset A2A3A3 PC card. The reset signal is augmented by a voltage obtained from the AR2 amplifier output, as mentioned above. This added voltage effectively shortens the time constant of the R64–R61–C1 network on the preset A2A3A3 PC card, and thereby assures that the retuning process at the high end of the pump VCO range (band 6) always starts at the lowest frequency within the band. The reference frequency from the 1–6 MHz VCO is applied through buffer amplifier Q1 and transformer T1 to a diode bridge phase detector consisting of diodes CR1 through CR4. The difference video signal appearing at terminal E48 is amplified by transistor Q2, and is also applied (through transformer T2) to the diode bridge. The detector output at terminal 5 of T2 is a dc voltage proportional to phase error. RF components of the signal are removed by the C9, R22, R23, and C11 network. Second harmonic components due to heterodyning of 1-MHz signals appearing at E47 and E48 are eliminated by L1 and C10, which form a 2-MHz trap circuit. If the loop is locked, the voltage at T2–5 is either a steady level or is varied slightly as needed to maintain phase lock. These variations appear at pin 2 of differential amplifier AR1. The resultant varying output at AR1–6 is applied via E41 to the hf VCO varicap CR1 (fig. FO–24) as the fine-control (phase) voltage. The dc signal appearing at resistor R23 is also applied to a ramp-generator circuit and to pin 2 of the fine-error differential amplifier (AR1). The ramp generator circuit consists of amplifier Q4, unijunction transistor Q5, and associated components. The

ramp generator is quiescent as long as the varying voltage at transistor Q4 input is below a frequency of a few Hz since high-pass circuit R28–C18 does not pass slowly varying signals. If the loop is not locked, the signal at R23 is an ac voltage having large frequency variations. The frequency is proportional to the frequency difference between the 1–6-MHz reference signal and the difference video signal. The resulting differential voltage, which is applied through transistor Q3, resistor R28, and capacitor C18 to the ramp generator, is then sufficient to exceed the threshold of transistor Q5. The slope of the ramp is determined by resistor R32, capacitor C29 and associated components in the circuit of transistor Q5. The ramp voltage at capacitor C29 is fed to pin 3 of differential amplifier AR2 to provide a sweep signal at the AR2 output. This signal sweeps the pump VCO signal through the phase-locked loop acquisition range to ensure phase-lock after frequency-lock has been accomplished. The dc balance of AR2 is set by potentiometer R50. Since the bandwidth or error correction range of the phase loop is small compared to that of the frequency loop, a stabilizing circuit is incorporated to coordinate the two. This circuit, an rc network composed of R24, C13, and R25, connects the phase error channel at differential amplifier AR1 with the frequency error channel at AR2. If the phase loop is excessively unbalanced during tuning or transients, the network couples part of the large phase error correction voltage to the frequency channel differential amplifier. This voltage actuates the frequency correction circuits for quicker stabilization of the correction loops. Conversely, during frequency correction, a portion of the relatively large error voltage developed by the frequency discriminator is applied to the phase-loop. The sense of the voltage is such as to drive the phase loop circuitry in the proper direction to null out the error once it is within the acquisition range of the phase-error correction loop.

(*c*) *Hf (pump) VCO preset A2A3A1.* The VCO preset circuit A2A3A1 (fig. FO–26) develops a dc-control level that enables the hf VCO to operate in a selected portion of the 88.999–61-MHz spectrum. The control level is determined by voltage dividers in a series of gating circuits connected to the coarse error control bus. Changes in the control bus level in effect vary the inductance in the hf VCO oscillator (fig. FO–24). Six nearly identical, two-transistor gating circuits are used to cover the spectrum in six bands. The gages are energized from the frequency select circuits by the same digital control inputs that select the output of the comb filter in the harmonic generator mixer circuit (fig. FO–23). *For example,* if the desired frequency is in the range of 61–63.999 MHz, the control logic will select band 6 and the signal is applied to terminal E25. This signal will saturate transistors Q11 and Q12. The voltage divider chain consisting of R59, CR12, R63, R61, CR6, R57, and R55 has a ground potential termination at the junction of R54 and Q11, and a +20-volt potential at the junction of R55 and Q12. Potentiometers R57 and R59 are adjusted to set the levels for the low and high ends of the band respectively. The diodes in the band-gating circuits isolate the active circuit from those circuits not gated on. The coarse-error voltage present on the control bus will now be scaled at the junction of R63–R64 by the voltage supplied by the two dividers. The other five bands operate in a similar manner.

(*d*) *In-lock detector A2A3A3.* The in-lock detector circuit A2A3A3 (fig. FO–27) provides an indication of whether the hf and 1–6-MHz VCOs are in phase-lock. In addition, when phase-lock is broken, this module provides outputs which initiate a retuning cycle. Inputs are applied to the indicator circuit from the 1–6-MHz VCO phase detector control loop at terminal E2, and the digital tune enable circuit at E3. The signal appearing at terminal E2 is applied to the base of transistor Q7. The output of transistor Q7 is combined with the signal appearing at terminal E8 from the hf VCO control loop, and applied through amplitude detector diode CR1 and its associated biasing and filtering circuits. If the input at either terminal E8 or E2 is an ac signal, which indicates absence of phase-lock, the net result is that a positive charge appears on capacitor C4. If both inputs are steady dc, no voltage is developed to charge capacitor C4. The voltage developed at capacitor C4 is also affected by the signal appearing at terminal E3 from the digital tune enable circuit. This signal is a momentary ground applied to the base of transistor Q6. When the digital tune enable signal is applied, the R1–C1 circuit discharges in accordance with its time constant. Transistors Q6 and Q2 then produce a positive voltage which charges capacitor C4 to approximately +20 volts. This voltage is applied through transistor Q3 to the base of transistor Q4 and holds relay K1 in the deenergized position. Capacitor C4 normally is discharged at the end of the 1-second period unless it is still receiving an ac (out-of-lock) signal. If capacitor C4 has

not discharged at the end of the tuning period, the voltage on capacitor C4 is still positive and will hold relay K1 in the deenergized position. The positive step at relay K1 pin d is applied through terminal E9 to the hf VCO coarse frequency control loop where the leading edge of the signal is differentiated to provide the low frequency reset signal. When relay K1 deenergizes, it also supplies a ground through contacts f and g as a digital tune-in-progress (DTIP) signal and applies a ground through contacts d and e and resistor R11 to the negative side of capacitor C5. This causes capacitor C5 to discharge through resistor R11 and the base of transistor Q5. Transistor Q5 then saturates holding transistor Q6 on through diode CR6 in a latching action. Resistor R18, capacitor C7, and resistor R12 provide timing for transistor Q5 conduction. When the phase loop error is reduced to zero and the 1-second delay is completed, transistor Q4 conducts and relay K1 is energized. The DTIP signal applied to terminal E7 is routed through contacts 6 and 7 of main power circuit relay K301 to the mode and status panel (7A5/7A12). When no power is applied to the transmitter, this indicator line is interrupted, and even though relay K1 is deenergized because of no primary power, the ground supplied by relay K1 will not result in an out-of-lock indication on the mode and status panel (7A5/7A12).

(2) *5-MHz amplifier A2A1* (fig. FO–28). The 5-MHz sine wave signal is routed from J2501 to the base of input amplifier Q1 via an impedance matching low-pass filter and isolation network. In the –1 and –2 configurations, the network consists of L8, C12, C13, C1, and R1. In the –3 configuration, the input amplifier is Q2 and an emitter-follower (Q1) is included for greater isolation. Losses introduced by the filter network are compensated for by the Q1 biasing network composed of R4, R2, and CR1. The diode raises the dc level of the signal, and Q1 is operated in class-C to provide an output of approximately 18 Vac for a small input signal. The Q1 output is applied through transformer T1 and a bandpass filter to snap-action diode CR2. This device acts as a nonlinear load and generates sharp pulses on the positive half-cycles that are rich in harmonics of the 5-MHz input. The output consists of a burst of pulses at 5-MHz intervals with sufficient drive to actuate ringing circuits in the comb filter of the harmonic selector. This 5-MHz spectrum signal is coupled through a high-pass filter, which passes only harmonics above 65 MHz to the harmonic selector via connector J2502.

(3) *Harmonic generator.* The harmonic generator (fig. FO–29) consists of a harmonic selector (A2A2), video amplifier and mixer (A2-A2A3), buffer amplifier (A2A2A2), and logic control (A2A2A1). The generator module performs three primary functions:

- Converts a 5-MHz reference signal from the master clock into a series of harmonics at frequencies of 65, 70, 75, 80, 85, and 90 MHz.
- Supplies a fixed 90-MHz signal output to the second L.O. RF section.
- Mixes a selected harmonic signal with an input from the hf (pump) VCO in the 88.999–61-MHz range to yield a variable output between 1.001 and 6.0 MHz.

(*a*) *Harmonic selector A2A2.* The harmonic selector (A2A2), (fig. FO–30) is composed primarily of six channels that are energized by +4-volt signals applied from band select circuits in the frequency select section. Pins A through F of connector J2212 are mixer injection select inputs for the 90-, 85-, 80-, 75-, 70-, and 65-MHz channels respectively. These signals are routed through the logic control module to provide switching for the channel circuits. Each channel contains a transistor switch, diode gate, ringing circuits and emitter follower. A seventh channel continuously passes 90-MHz components from the 5-MHz amplifier through the ringing circuit and emitter-follower Q1 to the second L.O. RF section. The channel circuits function overall as a comb filter for the mixer injection frequencies. The selected band select output provides continuity for the 5-MHz spectrum into the desired channel, and switches on the output transistor of that channel. *For example,* the 65-MHz injection select signal from the band control (A16) appears as a positive dc voltage at J2212–F of the harmonic selector (A2A2) module. It sistor of that channel. *For example,* the 65-MHz switching circuit of the logic control (A2A2A1) module. This signal is applied via R24 and R18 to the base of Q6, the collector of which is tied to +20 V through R6. As long as Q6 is nonconducting, CR6 is back-biased since its terminals are connected to the +20 V bus through R1 and R8 respectively. When Q6 is switched on by the band control signal, CR6 is forward-biased and provides continuity for the 5-MHz spectrum signal. This action does not affect the other diode gates, which remain back-biased and prevent passage of the 5-MHz spectrum signal to their respective channels. At the same time, the switching signal appearing at E14 is applied via R30 as a bias-on

voltage to Q7. This enables Q7 and provides a path for the 65-MHz harmonic component developed within the channel. The signal output from transistor Q7 is applied to the video amplifier and mixer A2A2A3 via E4.

(*b*) *Buffer amplifier A2A2A2* (fig. FO–31). The 88.990–61-MHz signal appearing at connector J2211 is applied through terminal E2 to the buffer amplifier. This module has two tuned stages providing gain for the signal and isolation between the pump output and the processing circuits of the hf phase-locked loop. The signal is introduced to the base of amplifier Q1. The output of transistor Q1 is applied through tuned transformer T1, amplifier Q2, and tuned transformer T2 to the mixer portion of the video amplifier and mixer (A2A2A3).

(*c*) *Video amplifier and mixer A2A2A3* (fig. FO–32). The signals appearing at terminals E1 and E3 of the video amplifier and mixer (A2A2A3) are processed through the decoupling networks in the base and emitter of mixer stage Q1 to remove undesired frequency components. The output signal appearing at the transistor Q2 emitter is in the range of 1.001 to 6.000 MHz. Zener diode CR1 stabilizes the transistor bias voltage to prevent transients in the dc line from affecting the mixer output signals. A three-stage video amplifier consisting of transistors Q3, Q4, and Q5 provides an output that is flat over the entire range. A limiting network is the base of transistor Q5 assures that the output signal appearing at connector J2215 is of nearly constant amplitude. This signal is that the 1–6-MHz difference video output supplied to the hf VCO phase detector and frequency discriminator circuits in the hf VCO control loop.

(*d*) *Logic control A2A2A1* (fig. FO–33). The logic control (A2A2A1) contains the switches that control the diode gates of the harmonic selector (A2A2) (fig. FO–30). Operation of the logic control circuits is described in connection with the harmonic selector (A2A2) previously discussed.

(4) *1–6-MHz VCO loop.* Since the pump VCO is locked to the 1–6-MHz reference signal (fig. FO–23), pump tuning can be accomplished by varying the 1–6-MHz-VCO frequency. A combined frequency and phase correction network controls the 1–6 MHz VCO. In this network, the output of the 1–6 MHz VCO is counted down to a convenient frequency (1 kHz) and then compared with a reference signal derived from the master clock. The purpose of the comparison is to produce an error voltage to hold the VCO at the proper frequency. To accomplish this, a sample of the VCO output is fed through a buffer amplifier to the VDSP divide-by-N divider (fig. 2–11). The VDSP is a variable divide-by-6000 counter whose division ratio is determined by the particular pattern of voltages on sets of lines (34) that have been actuated by the frequency select circuits. The division ratio is selected to give a 1-kHz output if the 1–6 MHz VCO is operating at the correct frequency for tuning the pump to the desired frequency. Changing the division ratio requires a corresponding change in the 1–6-MHz VCO frequency to produce a 1-kHz output. This change in the 1–6-MHz frequency affects the pump VCO which results in retuning of the transmitter. The nominal 1-kHz output of the VDSP (fig. FO–23) is supplied to one-shot multivibrator for pulse standardization. The one-shot output is applied simultaneously to the 1–6-MHz VCO phase detector and to the frequency discriminator. In the phase detector, the VDSP output samples a 1-kHz ramp reference signal derived from the master clock divider 1-kHz output. When the VDSP output is approximately 1 kHz, the time during which the reference voltage is sampled is governed by the relative phase of the VDSP output frequency and the reference. Variations in phase give rise to a varying dc (fine error) signal which is combined with a reference dc level is a summing network. The output of the summing network is applied to a differential amplifier-integrator where it is combined with the output of the frequency discriminator. The fine-error signal is also applied directly as a control signal to the 1–6-MHz VCO. The direct connection has a relatively fast response which, when the loop is in phase lock, rapidly damps loop noise or small drifts in the VCO frequency. The differential amplifier output is an integration of the combined fine- and coarse-error signals. Hence its response to loop variations is slower than the direct connection but its gain is much greater. Thus it has a greater effect on the process of bringing the loop into a locked state. The output from the VDSP is also used to produce a coarse-frequency control voltage. If the 1–6 MHz VCO is not on frequency, the output of the VDSP will be some frequency other than 1 kHz. Such frequencies cause an analog-type frequency discriminator circuit to yield a coarse-error voltage which is also applied to the differential amplifier. As indicated above, the coarse- and fine-error voltages are combined by the dif-

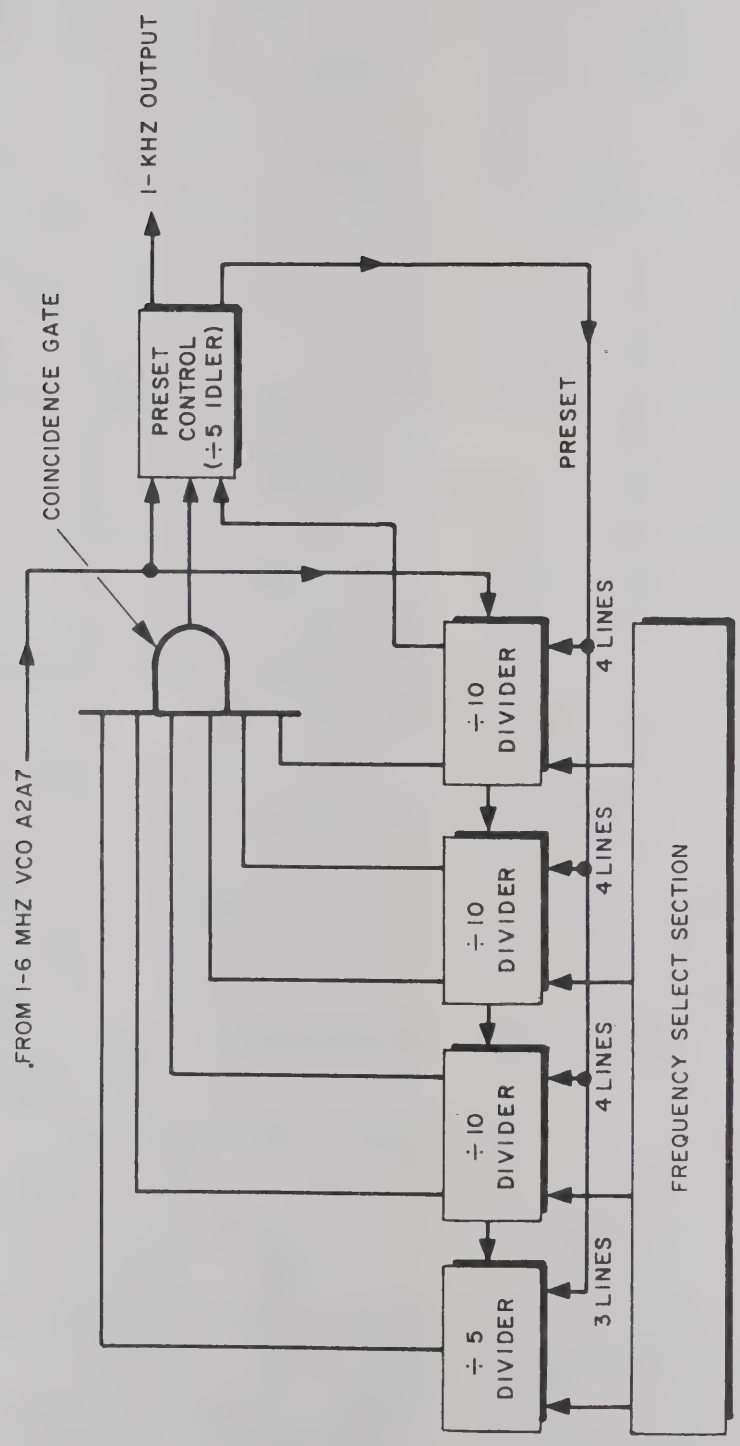


Figure 2-11. 1-6-MHz VCO variable (+N) divider A2A6A1, block diagram.

ferential amplifier to produce the 1–6-MHz VCO correction signal.

(*a*) *1–6 MHz VCO A2A7.* The output range of the 1–6 MHz VCO (A2A7) (fig. FO–34) is obtained by a band selection and tuning process which controls an oscillator operating in the 3–6-MHz range, and a divider circuit in the oscillator output section. The oscillator, FET Q1 is tuned by a LC tank circuit. Transformer T1, which is permanently in the VCO circuit, tunes the oscillator over the range of 3.001 to 3.8 MHz. Operating relay K1 inserts inductor L1 in parallel with transformer T1 to provide a tuning range of 3.801 to 4.8 MHz. Alternatively, relay K2 inserts inductor L2 is parallel with L1 to provide a tuning range of 4.801 to 6.0 MHz. Divider Z1 and gate G1 in the collector of amplifier Q3 act in combination as a divider with selectable divide ratios of 1, 2, or 4.

1. The frequency of the VCO is varied by coarse- and fine-control voltages and the band select signals noted above. The input signal appearing at pin J of connector J6101 is generated within the 1–6-MHz VCO phase-lock loop. The input signal at J6104 is the fine-error control voltage also generated in the loop. These two signals are applied to diodes CR1, CR2, and CR4, which control the resonant frequency of the oscillator tank. These diodes have a characteristic capacitance which varies with frequency, so that they act effectively as variable capacitors (varicaps). Transistor Q1 functions as an oscillator with the output of its tank circuit coupled to amplifier Q2. This stage is an isolated gate field effect transistor (IGFET), selected to provide minimum loading of Q1. Band select signals appearing on pins E and A of connector J6101 cause actuation of relays K1 and K2 respectively. Relays K1 and K2, in turn, control the insertion of inductors L1 and L2 to determine the frequency range of the oscillator. All input lines of J6101 are filtered by identical capacitors and inductors. These networks are not used in the –1 and –2 configurations, but are used in subsequent versions.

2. The output of amplifier Q2 is applied to the base of squaring amplifier-driver Q3. The frequency appearing at the collector of Q3 is applied as a clock pulse to pin 1 of divide-by-K divider Z1 and to pin 2 of AND/NOR gate G1. Divider Z1 is a dual (divide-by-two/divide-by-four) flip-flop with both of its outputs (pins 12 and 9) fed to gate G1. Divisor select signals appearing on pins K, H, or C of connector J6101 are also applied to gate G1 (pins 3, 5, or 10). These signals, combined with the outputs of divider Z1, determine whether the Q3 output is divided by 1, 2, or 4. To obtain a ÷1 condition, for example, the following sequence occurs. The signal at the Q3 collector is used at G1–2 as a direct clock input to the second AND gate of G1. When the ÷1 enabling voltage at J6101–K appears at G1–3, the AND gate conducts resulting in a high at the NOR gate output (G1–8). To obtain a ÷2 condition, the Q3 output is used at Z1–1 as a clock pulse for the left-hand flip-flop of Z1. The output of Z1–12 is routed to G1–4 as an input signal to the third AND gate. Since the ÷2 input at J6101–H is present at G1–5 as an enabling signal, and since the clock at G1–2 is ineffective at this time, the output at G1–8 appears only half as often as the clock at A1–1. Similarly, to obtain a ÷4 condition, the signal output of the first flip-flop (Z1–12) is used as a clock input to the second (right-hand) flip-flop. The output at Z1–9 is routed to G1–9 as an input signal to the fourth AND gate. Again, with the ÷4 input at J6101–C applied to G1–10 as an enabling signal, and with the clock signals at G1–2 and G1–4 now ineffective, the output at G1–8 appears only one-fourth as often as the clock signal at Z1–1.

3. When the band and divisor select signals from the frequency select circuits are combined, they produce an output in the 1–6-MHz range which is applied through connector J6102 to the hf VCO and to transistor Q4. This stage is a transistor switch that provides a buffered output to the VDSP.

(*b*) *Variable divider-synthesizer pump A2A6A1.* The variable divider synthesizer pump (VDSP) (A6A6A1) (fig. FO–35) counts down the 1–6-MHz VCO output signal to a frequency that can be conveniently compared with a reference signal. It consists of a divide-by-6000 counter, output coincidence gate, and divide-by-5 idler. The counter, composed of three divide-by-10s and a divide-by-5, receives input (clock) pulses from the 1–6 MHz VCO. The coincidence gate circuit is arranged to sense the 5994th count, after which an enabling signal is applied to a ÷5 idler. The idler performs the following functions: it provides a data strobe at the 5996th count to read in presets to the counter; it holds the counter effectively disabled for the next 4 counts; and it supplies pulses to the 1–6-MHz VCO circuit for sampling by the phase detector. If the divide-by-6000 counter were operated without the preset function, it would continuously divide by 6000. Since it is used as a variable divider, however, a

number related to the desired division ratio is preset into the counter in coded form. The division ratio is determined by control inputs from the frequency select circuits. The division ratio is selected to give a 1-kHz output when the 1–6 MHz VCO is operating at the correct frequency. Changing the division ratio causes a corresponding change in the 1–6-MHz VCO frequency to produce the 1-kHz output.

1. The time in which the divide-by-6000 counter reaches the 5994th state depends upon its initial state. If the counter were to start from state 0000, it would require the full 5994 pulses in order to produce the 5994th state at the coincidence gate. Owing to the use of the presets, however, counting is not necessarily initiated from the zero state. The presets may be any number between 0000 and 4999, corresponding to division ratios between 6000 and 1001. The preset numbers are inversely related to the division ratio, which in turn depends on the tuning frequency digits. The digits selected on the frequency select panel (7A4/7A11) are encoded in the frequency select circuits. The main divide-by-6000 counter includes three integrated circuit divide-by-10s (D2, D3, D4), and one integrated circuit divide-by-8 (D1), which is used as a divide-by-5. The internal functions of the decade counters are shown in the inset for the type N8280A device (fig. FO–35). The individual binaries internal to the device are identified as A, B, C, and D, corresponding to the QA, QB, QC, and QD notation at their respective outputs. The arrangement for D4 is modified slightly in that input binary A (connected directly to clock input pin 8) is not used. Instead, this input function with associated NAND gates is provided by F3 and associated NAND gates G2–C and G2–B. The external flip-flop is used instead of the internal binary D4–A because it operates more quickly, and therefore is preferable at the higher speeds required for the least-significant place digits. Thus the ÷N pulse appearing at J2801–14 is applied to the clock input (pin 12) of F3. The Q output at pin 8 of F3 is then applied to pin 6 of D4, where it serves as the clock input to internal binaries B and D. The individual decade binaries are connected internally in a combination ripple-through and synchronous arrangement, to provide a single output for each 10 input pulses. Similarly the divide-by-5 binary (D1) provides a single output for each five input pulses. (The internal arrangement for the divide-by-5 is shown in the inset for the N-8281 device (fig. FO–35).) The internal binaries of the four counters are of the J–K type, with their K terminals permanently high.

2. Each of the divide-by-10s counts from binary 0 (0000) to binary 9 (1001), then restarts at binary 0. The transition from a 9-count to a 0-count causes the output clock pulse, which is a negative-going transition at the QD output (pin 12). The main counter is a ripple-through type; the output of D4 is applied to D3 as the clock input; the D3 output is applied to D2, and the D2 output to D1. Thus, for each 10 pulses from J2801–14 to input pin 12 of F3, one pulse is applied via pin 12 of D4 to D3–8. For each 10 pulses from D3–12 applied to D2–6, one pulse is applied via D2–12 and D1–6. The latter, a divide-by-5 contains four binaries of which only B, C, and D are used (see fig. FO–35 for N8281A device). In this counter arrangement, the binaries can count up to 6000 states, the last being the same as the 0000 state. The digital inputs applied from the frequency select circuits through J2801 contain the desired divide ratio for the presets, and are in nines-complement BCD form. The units of-kHz codes are applied through pins S, P, and R to D1; the 100s-of-kHz through pins, L, 11, M, and K to D2; the 10s-of-kHz through pins 5, H, E, and D to D3; and the units-of-kHz through C, B, and A to D4 and –2 to gate G2–C. Since the input codes to the divide-by-10s are of four digits each (see truth table, fig. FO–35), the codes applied to pins K, D, and 2 are the least significant digits for their respective devices. The codes are strobed into the counter devices during the preset cycle, and determine the initial count from which the devices start after preset. *For example,* if a 3 preset into D3 (0011) after six clock pulses from D4, an output from D3 would be applied to D2. However, thereafter until the next pulse, D3 requires 10 inputs from D4 to produce an output to D2. Assume that initially all four counters are in the 0 state (corresponding to a preset of 0000), and that the idler has completed its cycle, with F2, F1–A, and F1–B also in the 0 state. When F2 is in the 0 state, the $\overline{Q}$ output from F2–6 enables the J and K inputs of F3. Since F3 is a J–K flip-flop, enabling the J and K inputs permits F3 to toggle back and forth with each succeeding clock pulse. The first clock pulse at J2801–14 is applied to F3–12, causing a high output at F3–8. F3–8 remains high until the second clock pulse at F3–12. The effect of the second and subsequent clock pulses (through count 10) is shown in table 2–6.

3. The action of counters D3 and D2 is similar to that of D4 except that the functions of

Table 2-6. VDSP Timing Chart No. 1

Count	Location	Event
0		All binaries in zero state
1	F3-12	F3-Q → high
2	F3-12	F3-Q → low
	D4-6	D4-B clocked; QB → high One input to internal gate → high.
	D4-C	D4-C (no effect)
	D4-D	D4-D (no effect)
3	F3-13	F3-Q → high
4	F3-12	F3-Q → low
	D4-6	D4-B clocked; QB → low; internal gate input → low.
	D4-C	D4-C clocked; QC → high; gate input → high but other gate input still low.
	D4-D	D4-D clocked; no effect
	D4-2	QC outputs to G1-5; no effect
5	F3-12	F3-Q → high
6	F3-12	F3-Q → low
	D4-6	D4-B clocked; QB → high; gate high.
	D4-C	D4-C (no effect)
	D4-D	D4-D no effect because gate not high when clock pulse occurred.
7	F3-12	F3-Q → high
8	F3-12	F3-Q → high
	D4-6	D4-B and D4-D clocked; QB → low, gate input → low.
	D4-C	D4-C clocked; QC → low; gate input → low.
	D4-D	D4-D → clocked; QD → high; J input to D4-B → low; high to D3-8, no effect.
9	F3-12	F3-Q → high
10	F3-12	F3-Q → low
	D4-6	D4-B and D4-D clocked; QB no effect because J input low; gate input stays low.
	D4-C	No effect
	D4-D	D4-D clocked; QD → low; D3-8 clocked; J input to D4-B → high.

F3, G2-C, and G2-B are provided by elements within the decade units. Divide-by-5 counter D1 operates in essentially the same way as the decade counters. In this case, however, the clock input is applied from D2-12 to D1-6, bypassing the A binary. As stated previously, the circuit of coincidence gate G1 is arranged to sense the 5994th counter, after which it supplies an enabling signal to the idler circuit. In order for G1 to sense the 5994th count, the Q output of D4 at its 4th count must be high and present at G1 at the same time as the Q outputs of D3, D2, and D1 at their 9th, 9th, and 5th counts respectively. This condition is met when highs appear at the following outputs of the counter:

- D1-12 and D1-9—corresponding to a BCD 5 in the D1 counter (1001). These outputs are applied to G1-12 and G1-11 respectively.
- D2-12 and D2-5—corresponding to a BCD 9 in the D2 counter (1001). These outputs are applied to G1-1 and G1-2 respectively.
- D3-12 and D3-5—corresponding to a BCD 9 in the D3 counter (1001). These outputs are applied to G1-3 and G1-6 respectively.
- D4-2—corresponding to a BCD 4 in the D4 counter (0100). This output is applied to G1-5.

When coincidence occurs, G1 passes a low to inverting gate G2-A for routing to the J gate of idler counter F2. The other input to the F2 J gate (pin 5) appears at the time of the next high at F3-8. This occurs at the next count (5995). At this point the J and K gates of F2 are both high. The next pulse (5996) at J2801-14 triggers F2, and causes F3 to go low. The effects of the 5996th and subsequent pulses appearing at J2801-14 are shown in table 2-7. A forbidden state of the idler logic is one in which F2 is low at the same time that F1-A and/or F1-B are high. To prevent this condition, NAND gate G2 is incorporated. Should F1-A and/or F1-B be high when F2 is low, the gate conducts, supplying the reset pulse to F1-A and F1-B, and preventing the idler from blocking.

Table 2-7. VDSP Timing Chart No. 2

Count	*Event*
5996	F2 goes high and F3 goes low. F2 Q output disables F3 input and strobes presets into D4, D3, D2, and D1. Preset removes coincidence from G1 and disables J input to F2. F2 output enables J and K inputs to F1-A and strobes presets F3 via G2-B or G2-C.
5997	F1-A Q output goes high, enabling F1-B J and K inputs.
5998	F1-A Q output goes low, and F1-B Q goes high. F1-B Q output is applied to loop phase detector, and F1-A Q output disables J and K inputs to F1-B.
5999	F1-A goes high and F1-B remains high. F1-B Q output and F1-A Q output enable K input of F2.
6000	F2 goes low, disabling J and K inputs to F1-A
or	F2 Q output goes high, causing—
0000	(a) Removal of preset strobe from

Count	*Event*
	D4, D3, D2, D1, G2–C and G2–B
	(b) Enabling of J and K inputs to F3 so that next clock pulse can initiate new cycle
	F1–A goes low, disabling J and K inputs to F1–B and K–11 input to F2.
	F1–B goes low, ending output to phase detector and disabling K–9 input to F2.

(*c*) *1–6-MHz phase lock loop A2A6A2.* The 1–6-MHz phase lock loop (A2A6A2) (fig. FO–36) generates three signals: a 1–6 MHz VCO error signal, a fine-control signal, and a coarse-control signal. The fine- and coarse-control signals are applied to the 1–6-MHz VCO and the error signal is applied to the in-lock indicator circuit in the hf VCO. The 1-kHz reference signal from the master clock divider (A2A5A1) is applied through pin 2 of connector J2802 to the ramp generator consisting of Q5, Q6, and associated components. When the square wave is applied, Q6 conducts during the positive portion and its collector approaches ground potential. When the pulse goes negative, current source Q5 conducts, charging C19 through R6. The ramp slope corresponds to the charging rate. The output of Q5–Q6 is applied to the drain of field-effect transistor (FET) Q1. Transistor Q1 samples the ramp output periodically and yields a dc output at capacitor C5. When the inputs of Q1 are phase-locked, the ramp is sampled at the same point on successive cycles and the signal at C5 is essentially constant. If the loop is not frequency-locked, the ramp is sampled at different points on each cycle and the dc level at C5 changes. These voltage level variations are applied to FET Q3, which has a high input impedance and thus does not disturb the sample-and-hold circuit. The output of Q3 is applied to buffer amplifier Q4 and to differential amplifier device A1. The output of Q4 is applied through pin 13 of connector J2802 to the hf VCO as the 1–6-MHz VCO error signal. The output of Q3 is also applied to the 1–6-MHz VCO control circuits through pin 4 of connector J2802. The nominal 1-kHz signal from the VDSP is applied through pin 11 of connector J2802 to a pulse-counting frequency discriminator consisting of Z1, R11, and C10. Z1 is a one-shot whose output pulses are used for coarse- and fine-correction signals respectively. The negative-going output pulses appearing at pin 11 of Z1 are applied to the base of isolation stage Q2, and the output of Q2 is coupled across C6 to the gate input of FET Q1. The tuning characteristics of the pulses are determined by C4 and R8. The pulse rate depends upon the VDSP input frequency and in turn determines the rate at which Q1 samples the voltage on C19. If the loop is out-of-lock, the fine-control error voltage applied to Q3 varies; if in-lock, the voltage is a steady dc. The Q3 output is routed via J2802–4 to the 1–6 MHz VCO as the fine-error signal, and via isolating amplifier Q4 and J2802–13 as the in-lock indicator error signal. The positive-going pulses appearing at Z1–4 are integrated in the R11–C10–R18 network and applied to input pin 7 of differential amplifier A1. The output at A1–2 is applied via J2802–14 as the coarse-control signal to the 1–6 MHz VCO. Capacitors C13 and C20, in conjunction with resistors R20 and R21, limit the gain of A1 at higher-error signal rates to provide frequency stabilization.

c. L.O. Signal Generating Section. The L.O. signal generating section consists of the second L.O. RF section A2A4 (fig. FO–34) and the second L.O. variable divider A2A5A2 (fig. FO–36). In addition, RF box No. 1 A2A5 (fig. FO–37), RF box No. 2 A2A6 (fig. FO–38), and filter box A2A8 (fig. FO–39) are also included in this section.

(1) *Second L.O. RF section A2A4* (figs. FO–37 and FO–38). The second L.O. RF section (A2A4) operates in conjunction with the second L.O. variable divider (A2A5A2) to develop the L.O. signal for the RF translator (A1). Inputs include reference signals from other portions of the frequency synthesizer (A2), and divisor select signals from the 100s-of-Hz portion of code conversion matrix No. 2 (A18). The first loop includes a 9.1-MHz voltage-controlled crystal oscillator (VCXO), mixer, shaper, second L.O. variable divider circuit, and a phase detector. Buffer amplifiers are used in the outputs of the 9.1 MHz VCXO and the mixer. The 9.1001–9.1010-MHz output of the VCXO is applied via a buffer amplifier to a second mixer, where it is heterodyned with a 10-MHz injection signal from the frequency injection select circuit. The output of the second mixer is the difference frequency component—a signal in the 0.8990–0.8999-MHz range. This signal is applied through an 899-kHz amplifier to a balanced phase detector. This stage is part of the second phase-locked loop consisting of the phase detector, a differential amplifier, a 90.899X MHz VCXO, a third mixer, and two buffer amplifiers. This second loop provides precision control over the 90.8990–90.8999-MHz second L.O.

output through its mixing and phase-comparison process. The third mixer heterodynes the 90.899-X signal with a 90-MHz reference signal from the harmonic generator (A2A2) to produce a 0.8990–0.8999-MHz difference frequency which is applied through the buffer amplifiers to the balanced phase detector. The output of the phase detector is compared with a dc reference in the differential amplifier to provide the 90.899X-MHz VCXO correction voltage.

(*a*) The purpose of the variable divider is to provide an output that can be compared in the phase detector to yield an error signal that will precisely control the 9.1 MHz VCXO. Since the precision control must be effected in 100-Hz steps, the variable divider is designed to provide a 100-Hz output when the VCXO is in phase-lock. Instead of operating the divider directly at the 9.1-MHz frequency, the phase-locked loop obtains the 100-Hz output by means of a precision reference signal of 100 Hz in conjunction with a ÷2000 counter operating in the 1001–1010 range.

(*b*) The basic generating element of the first phase-locked loop is a 9.1 MHz VCXO, the output of which is applied to the loop mixer. The 9-MHz input to the mixer is derived from the 1-MHz master clock reference, which is processed by a X3–X3 multiplier to yield a fixed 9-MHz signal. The output of the mixer is 100 kHz, with variations depending upon the frequency of the VCO. The nominal 100-kHz output is supplied through shaping circuits to the second L.O. variable divider (A2A5A2). The divisor for this circuit is a number ranging from 1001 through 1010. The exact division ratio is determined by the input frequency select signals, which are derived from the frequency select digit that occupies the 100-Hz position. If the digit is a zero, the division ratio is 1010; if the digit is a one, the ratio is 1009, etc., up to the frequency digit of nine, where the ratio is 1001. The output of the variable divider is compared in a phase detector with the 100-Hz ramp voltage produced by the clock section. The output of the phase detector in turn is the frequency control signal applied to the 9.1 MHz VCXO. When the VCXO is in-lock, it will have a frequency of 9.1001 to 9.1010 MHz as determined by the variable divider.

(*c*) The 9.1-MHz VCXO signal is applied to the mixer, the output of which continues to feed the control loop. As previously stated, the VCXO output is also applied in parallel to a second mixer, to which the 10-MHz injection signal derived from the master clock 5-MHz reference is also routed. After processing by a X2 multiplier, the frequency injection select is supplied as a stable 10-MHz signal to the mixer.

(*d*) The second mixer output is a frequency between 0.8990 and 0.8999 MHz. Since the inputs consist of a fixed 10-MHz signal and a selected discrete signal from the 9.1 MHz VCXO, the mixer output is available in 10 discrete steps. Furthermore, each step corresponds to one of the four last-place numbers of the signal that will finally appear as the second L.O. signal. To accomplish the required combining operation, the mixer output is routed first through an 899-kHz amplifier and then applied to the second control loop. The input to 9.1 MHz VCXO Q21 (fig. FO–38) is derived from the phase detector in the variable divider. The frequency of oscillator Q21 is controlled by crystal Y1 and two variable capacitors (varactors), CR1 and CR2. The capacitance of varactors CR1 and CR2 is controlled by the dc level supplied from the phase detector. Thus the VCXO frequency in effect is controlled by the variable divider. The 9.1-MHz output is applied through transformer T1 and buffer amplifier Q22 to a balanced mixer, which is composed of CR3, CR4, and associated biasing and filtering networks. Another input to the mixer is a 9.0-MHz reference signal derived from the 1-MHz reference output of the master clock section. This signal is applied through two tripler stages, Q25 and Q24, and then fed to the balanced mixer through C23 and C24. The mixer output is fed through buffer amplifier Q23 to the variable divider for the division and phase-comparison operations. The output at this point is a signal ranging from 100.1 to 101.0 kHz.

(*e*) The output of the 9.1 MHz VCXO is also coupled through buffer amplifier Q26 to the second balanced mixer stage, composed of CR5 and CR6 and associated circuits. The other input to the mixer is the 10-MHz injection signal developed by the X2 multiplier composed of Q29 and associated components. A 5-MHz reference signal from the master clock section is supplied to the multiplier through J3628 and permanently deenergized relay K1. (The switching functions of relay K1 are required only when the synthesizer is used with the receiver. In the transmitter application there is not energizing circuit for the relay coil; hence the normally-closed contacts provide a permanent routing for the 10-MHz signal.) The 10-MHz output is routed through relay contacts B3 and B2 to the second mixer. The mixer output is the difference

between 9.1 MHz VCXO and the 10-MHz injection signal. This output is amplified by 899-MHz amplifier (Q27) and fed via the bandpass filter to the balanced phase detector (CR10 through CR13). The 899-kHz signal is used as a reference to control the frequency of the second L.O. (Q9) which operates in the 90.8990–90.8999-MHz range. The L.O. signal is routed to output connectors J3630 and J3631 and also to the active mixer (Q15). It is heterodyned in the mixer with the 90-MHz injection signal from the harmonic generator (A2A2) and translated down to the 899.0–899.9-MHz range. This signal is applied via buffer-driver stages (Q14 and Q13) to the balanced phase detector (CR10 through CR13). Here it is compared with the 899-kHz reference signal from Q27, resulting in a dc-correction signal. This voltage in turn is applied to Q12, the signal input section of differential amplifier (Q10–Q12). The differential amplifier operating point is controlled by the reference voltage at the base of Q10. The output of the differential amplifier is applied to varactor CR19, where it provides vernier control over the tank circuits of VCXO Q9. The second L.O. output signal appears at J3631 and J3630 for routing to the RF translator (A1).

(2) *Second L.O. variable divider A2A5A2.* Operation of the second L.O. variable divider circuit (A2A5A2) (figs. FO–39 and FO–40) is similar to that of the VDSP except that the preset input is a 5-digit module-10 code like that of a binary shift register. It receives its input signal, which is approximately 100 kHz, from the second L.O. RF section (A2A4). This signal is processed by the squaring circuit and supplied to the divide-by-2000 divider as shown in figure FO–39. The divider counts the pulses, and, when it reaches the count of 1010, produces an output which triggers a blocking oscillator. The oscillator samples a 100-Hz ramp voltage which is fed to a diode bridge phase detector from the master clock section. The phase detector output, which is the VCO control voltage, is then applied through an emitter follower and loop filter to the second L.O. 9.1 MHz VCXO. At the same time that the 1010 count appears, an output is also supplied to the preset gates. The preset gates insert a number into the divide-by-2000 counter which causes it to function as a variable divider. The number set in is determined by the hundreds-of-Hz digit from code conversion matrix No. 2 (A18) in the frequency select circuits. The numbers set in range from zero through nine. If the hundreds digit is a zero, the counter is designed to divide by 1010. To accomplish this, the counter requires a zero preset. If the hundreds digit is a one, the counter must divide by 1009, and requires a one preset. The progression continues until the hundreds digit is a 9 when the preset number is 16, at which time the counter divides by 1001. The input signal to the divider at pin 6, from the VCXO in the second L.O. RF section, is fed initially to the shaping circuit. This circuit consists of tunnel diode CR1, which develops a sharp pulse, and Schmitt trigger Q1 and Q2, which generates the squared-output pulse. The output is supplied as the clock signal to the first band of divide-by-10 stages (flip-flops FF1 through FF5).

(*a*) Initially, assuming that all five flip-flops are in the zero state, the SQ input of FF1 is low (since it is determined by the output of FF5). The $R\overline{Q}$ input of FF1, which is determined by the G1B gate output, is high. This is due to the low level at pin 5 (which is tied to the output of FF5), and the low at pin 6 (which is tied to the output of FF4). Consequently, a one is read into FF1. The clock pulse does not affect FF2 through FF5 at this time because they are already in the zero state; i.e., the SQs are high and the $R\overline{Q}$s low. Hence a clock pulse applied at this time can only result in a redundancy. On the next pulse, the one in FF1 is transferred to FF2 and another one is set into FF1. On the third pulse, the one from FF2 is transferred to FF3, the one from FF1 is transferred to FF2, and FF1 receives another one. On the next (fourth) pulse, FF1 through FF4 all assume the one state. At this point the Q output of FF4 is high, which will affect the pin 6 input to gate G1B, but the Q output of FF5 is still low, so the output of G1B remains high. The next (fifth) clock pulse causes FF5 to assume the one state, along with FF4, FF3, FF2 and FF1. At this point the Q outputs of FF5 and FF4 are both high, causing the G1B output to go low, making the $R\overline{Q}$ input to FF1 also low. At the same time, the Q output of FF5 is high, causing the SQ input of FF1 to go high, which means that the next (sixth) clock pulse will cause a zero to be read into FF1. Therefore, on count six, the five stages assume the state 01111. The effect of succeeding pulses can be readily determined by examining the input to FF1. If on the next (seventh) pulse another zero is read into FF1, the binary word becomes 00111. On the eighth pulse the FF1 input remains unchanged, and the word is 00011. On the ninth pulse an-

other zero is read in, resulting in the word 00001. At this point, the Q output of FF4 goes low and both inputs to the G1B gate are also low. The resulting high output causes both the SQ and $R\overline{Q}$ inputs of FF1 to be high. When this occurs, the clock pulse has no effect and the stage remains in the present (zero) state. Therefore, on the next clock pulse, the word becomes 00000, corresponding to the original condition.

(*b*) When the divider is in count 9 (and only in count 9), both the $\overline{Q}$ output of FF4 and the Q output of FF5 are high. These levels are fed back to pins 4 and 3 respectively of G3A so that on the 10th input, when the first divide-by-10 section is reset to zero, a clock pulse may be gated through pin 2 of G3A to drive the subsequent counter sections. The clock pulses are inverted by G2A and applied to the second band of divide-by-10 stages. These operate in the same manner as the previous set. When they reach the nine state, the $\overline{Q}$ output of FF9 and the Q output of FF10 are supplied to G5B along with the output of G2A. Then, on the next pulse, the stages in the second set are reset to zero, and a clock pulse is applied through inverting gate G4B to the third bank of divide-by-10 stages. Like the first two dividers, the third divider produces an input at state nine which is fed through G5A and G4A as a clock pulse to FF16. The G4A output occurs once in every 1000 inputs to the variable divider. The Q output of FF16 is supplied as one input to G6. The other inputs to G6 indicate when the first divide-by-10 set is in the zero state, when the second divide-by-10 set is in the one state, when the third set is in the zero state, and when FF16 has been triggered. Thus, G6 indicates when a 1010 count has been reached. The next clock pulse from the shaping circuit is applied through pin 12 of G6 to clock the output into G4D. At the same time, it resets FF16, resets the second divide-by-10 (which had been in state one), and also causes an output from G4D to be supplied to the preset gates G1C, G1D, G1A, G2B and G2C. The Q output of FF16, which lasts for ten clock pulses, is supplied through C2 to the input of blocking oscillator Q3. The oscillator pulse causes a sampling through the diode bridge phase detector composed of CR5, 6, 7, and 8. The other input to the phase detector is the 100-Hz ramp signal. The sampled voltage is stored on capacitor C6. The stored level is transmitted through Q4 and the filtering network to the second L.O. RF section to control the 9.1 MHz VCXO.

d. RF Box No. 1 A2A5 (fig. FO–41) *and RF Box No. 2 A2A6* (fig. FO–42). For additional RF shielding, some of the frequency synthesizer circuits are inclosed in housing called RF box No. 1 and RF box No. 2. RF box No. 1 contains the second L.O. variable divider (A2A5A2) PC card and the master clock divider (A2A5A1) PC card. It also provides a mounting base for components of the low-pass filter utilized in the 100-kHz reference signal supplied to channel A1–B1 dual-balanced modulator A7. RF box No. 2 contains the variable divider synthesizer pump (A2A6A1) PC card and the 1–6-MHz phase-lock loop control (A2A6A2) PC card.

e. Filter Box A2A8 (fig. FO–43). The frequency synthesizer box accepts all inputs and routes them through capacitors and line filters to the applicable circuits. RF type connectors are provided for all RF-sensitive signal lines for both input and output signals.

2–15. Power Supply Analysis (fig. FO–5)

The main power source for the transmitter is 120 Vac, ±10%, 47–420 Hz. Control of the power is accomplished by the application of +28 Vdc through POWER ON/OFF switch S301, which controls relay K301. Thus, when the +28 Vdc is available, switch S301 is set to the ON position. This energizes relay K301, which then completes the 120 Vac circuit to the input of the power supplies. In addition, relay K301 completes the circuit to enable the system digital tune-in-progress indicator (SYS TUNING) on the mode and status panel (7A5/7A12). The system digital tune-in-progress signal is also routed through switch S301 to interrupt the SYS TUNING indication when primary power is not applied to the transmitter, thus preventing false tuning indications. Front panel indicator DS301 is illuminated when 120 Vac is applied to the three power supplies. One lead of the 120 Vac circuit to the power supplies is fused with fuse F301, a 1.5-ampere fuse in an indicating fuse holder (blown-fuse indicator). A second fuse (F302) is included in the input to the −28 Vdc power supply as additional protection. This fuse is rated at 0.5 ampere, and is also included in a fuse holder equipped with a blown-fuse indicator. The +28 Vdc utilized in the power supply turn-on control circuits is also routed to the frequency synthesizer (A2) where it is used to heat the temperature control ovens in the VCO circuits.

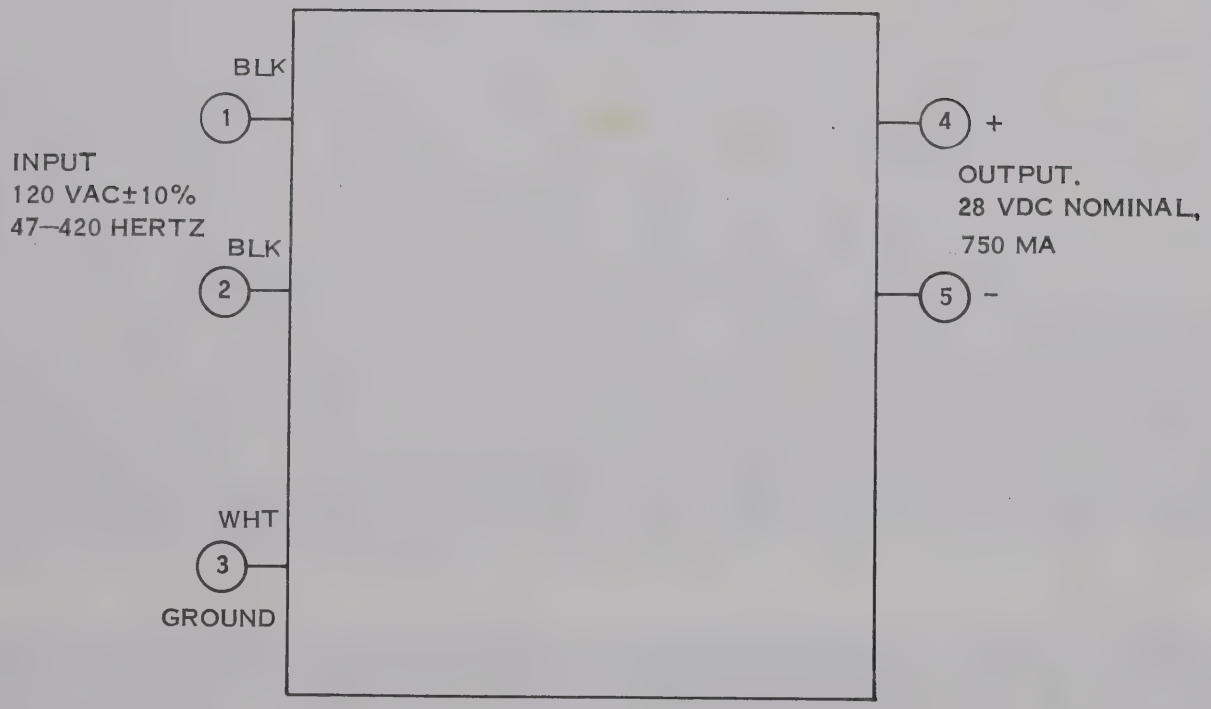
*a. Power Supply PS-1 (−28 Vdc) A19 (*fig. 2-12). Power supply PS-1 (unit A19) provides an unregulated −28 Vdc (+3, −10 Vdc) output at a maximum current of 0.750 ampere. Maximum ripple voltage on this output is 3 volts peak-to-peak, which is acceptable within the uses for this voltage. The −28 Vdc is supplied to the frequency synthesizer (A2), RF translator (A1), and to the signal control and transmit gain control circuits in the transmitter. The input 120 Vac is stepped-down through transformer T1, and rectified in a bridge rectifier composed of diodes CR1 through CR4. Filtering is accomplished by capacitor C1, and resistor R1 is a conventional bleeder resistor. The entire power supply is in a sealed, encapsulated assembly, and is not repairable. If a malfunction occurs within the −28 Vdc power supply, the entire unit is replaced.

b. Power Supply PS-2 (+20 Vdc) A11 (fig. FO-44) Power supply PS-2 (unit A11) provides a regulated output at +20 ±0.1 Vdc, at a maximum current of 1.5 ampere. Maximum ripple content of the output voltage is 3 mv peak-to-peak. Line voltage (input 120 Vac) variations of ±10% are regulated to create no more than a 0.05 percent change or ±4 mv maximum change in the output voltage. The output voltage (+20 Vdc) is used in the dual balanced modulator (A7), RF translator (A1), frequency synthesizer (A2), transmit gain control (A4), multiplex carrier generator (A9), tune-enable relay K301, the ACL circuits, and the signal control circuits.

(1) The circuitry for power supply PS-2 consists of an ac-input circuit and transformer, a bias supply for internal use consisting of an auxiliary rectifier, filter, and zener diode regulator; and a main supply consisting of the main rectifier and filter, a series regulator, an emitter-follower driver, an error signal amplifier, a current limit amplifier, a current sink, an output voltage sensing circuit, and an output current sensing circuit. Single-phase input power is applied to transformer T1 through the input circuit containing the thermostat (S1) which protects the power supply against overheating. The main rectifier is a full-wave bridge rectifier composed of diodes CR8-CR11. The rectifier provides the power which is filtered by capacitor C8, regulated by series regulator Q8, and delivered to the output. The bias supply (half-wave auxiliary rectifier CR7) provides voltage filtered by capacitor C7 and regulated by zener diode CR6 for current limit amplifier Q3 and error amplifier Q1 and Q2. Zener diode CR1 and resistor R5 across the bias supply provide a regulated temperature-compensated reference voltage. Operation of the voltage regulator circuit is determined by changes in the output voltage. A change in the output voltage is detected by sensing divider R1-R2-R3, which compares the output voltage with the reference voltage. This provides an error voltage at the junction of R2 and R3, which is amplified by error amplifier Q1 and Q2 and current-amplified by emitter follower Q5. The amplified signal from Q5 controls the voltage across series regulator Q8 which functions as the active regulating element restoring output voltage to the proper level.

(2) Current limit circuit operation is determined by changes in the load. Current limit amplifier Q3 samples load current through current-sensing resistor R14. When the voltage drop across R14 increases (compared with the preset regulated-voltage reference determined by R17, R18, CR4 and Q4), Q3 conducts. Thus, when the output current rating of the unit is exceeded, current limit amplifier Q3 conducts, decreasing the current through emitter follower Q5. This results in an increase of voltage across the series regulator and a decrease of the output voltage, effectively limiting the output current to a safe value. The current-limit value is determined by the factory setting of current-limit potentiometer R17. When operating conditions approach short circuit, and output voltage value decreases below the minimum voltage rating, current sink Q4 saturates, and divider R17-R18-Q4-R19 becomes purely resistive with no regulated reference for current limit operation. With Q4 at saturation, the voltage reference becomes proportional to the output voltage, decreasing as the output voltage decreases. This permits Q3 to turn on at lower load currents until output voltage decreases to zero and current decreases to a predetermined low value.

c. Power Supply PS-3 (+6.4 Vdc) A10 (fig. FO-45). Power supply PS-4 (unit A10) provides a regulated output of +6.4 ±0.05 Vdc at a maximum current of 1.5 ampere. Maximum ripple content of the output is 3 mv peak-to-peak. Output variations are held to 0.5 percent, with a maximum of ±4mv under input voltage variations of ±10 percent. Output load variations are regulated to 0.03 percent (maximum ±3 mv) over load variations ranging from 10 to 100 percent. The output is supplied to the mode and



NOTE:
REFERENCE DESIGNATIONS ARE INCOMPLETE.
PREFIX THE DESIGNATION WITH THE FOLLOWING
APPROPRIATE DESIGNATION:

PRIMARY TRANSMITTER	6A9A19
SECONDARY TRANSMITTER	6A11A19

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Figure 2–12. Minus 28 Vdc power supply A19, external connections.

status panel (7A5/7A12), transmit gain control (A4), frequency synthesizer (A2), carrier adjust local select switch S303, frequency select memory circuits, code conversion matrices, band control circuits, and the signal control circuits.

(1) The power supply circuits consist of an ac input circuit and transformer, a bias supply for internal use consisting of an auxiliary rectifier, filter, and a Zener diode regulator, and a main supply consisting of the main rectifier and filter, a series regulator, emitter follower driver, an error amplifier, a voltage amplifier, an OR gate, and an output voltage sensing circuit. Single-phase input power is applied to transformer T1 through the input circuit containing thermostat S1, which protects the supply against overheating. The main rectifier, a full-wave rectifier composed of diodes CR8–CR10, provides the power which is filtered by capacitor C8 and then regulated by a series regulator and delivered to the output. The bias supply, composed of half-wave auxiliary rectifier CR7, provides voltage filtered by capacitor C7 and regulated by zener diode CR6 for voltage amplifier Q3 and error amplifier Q1. Zener diode CR1 and resistor R4, across the bias supply, provide a regulated, temperature-compensated reference voltage. Operation of the voltage regulator circuit is determined by changes in the output voltage. A change in the output voltage is detected by sensing divider R1 and R3, which compares output voltage with the reference voltage. This provides an error voltage at the junction of R1 and R3, which is amplified by error amplifiers Q1 and Q3, and current-amplified by emitter follower driver Q5. The amplified signal from Q5 controls the voltage across series regulator Q8, which functions as the active regulating element, restoring output voltage to the proper level.

(2) Current limit circuit operation is determined by changes in the load. When load current increases above the rated current value, the voltage drop across current-limit potentiometer R14 increases, driving OR gate diode CR3, on, and OR gate diode CR5 toward cutoff. The resulting base current supplied to voltage amplifier Q3 drives Q3 toward turn-on. With Q3 conducting, the current to driver Q5 decreases, limiting the base current to series regulator Q8, resulting in an increase of voltage across the series regulator and a decrease of the output voltage. This effectively limits the output current to a safe value. The current-limit value (1.9 ampere) is determined by the factory setting of current-limit potentiometer R17. When operating conditions reach short circuit, the output voltage value decreases to zero, and the current decreases to a predetermined current-limit value and remains unchanged.

CHAPTER 3

DIRECT SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL MAINTENANCE INFORMATION

3-1. Introduction

This chapter provides the information necessary to maintain the transmitter at the direct support maintenance level. These maintenance instructions are primarily intended to assist the repairman in determining whether the equipment is operating properly, and if not, to localize the malfunction to a fault at the plug-in card or module level. The scope of maintenance is assigned by the maintenance allocation chart (MAC). Direct support (DS) level maintenance is performed by specially trained units in direct support of using organizations. Applicable publications authorize a large assortment of parts, subassemblies, assemblies, precision tools, and test equipment that is provided to using organizations to enable repair of subassemblies, assemblies, and the overflow from the lower categories within the limits imposed by the specified authorizations. When necessary, the lower categories are provided technical assistance, mobile repair crews, and repair parts by DS organizations. The maintenance information in this chapter includes troubleshooting procedures, adjustments, removal and replacement procedures, performance test procedures, and performance standards such as voltage and frequency measurements and waveforms. The order of presentation of this maintenance information is arranged in a sequence which is logical in terms of specific maintenance steps required to maintain the transmitter at the direct support maintenance level.

3-2. Detecting Faulty Operation

Transmitter performance tests (sec. IV) are provided for use in determining abnormal operation. Furthermore, indications of both normal and abnormal operation are given in the troubleshooting charts (sec. II). Voltage and frequency measurements and waveforms are also provided in section II of this chapter as a further aid in troubleshooting.

3-3. Locating Trouble

The following types of troubleshooting charts are provided to aid in locating trouble in a minimum amount of time.

a. Rack-Mounted Troubleshooting Chart. The rack-mounted troubleshooting chart (para 3-24*a*) enables the repairman to locate trouble based on indications obtained while the transmitter is functioning as part of the radio subsystem. The use of this type of troubleshooting is recommended prior to bench troubleshooting in order to minimize downtime.

b. Bench Troubleshooting Chart. The bench troubleshooting chart (para 3-24*b*) is designed to enable the repairman to locate trouble based on indications obtained while the transmitter is removed from the radio subsystem and connected to the receiver-transmitter test set (T3-24732A).

3-4. Checking Serviceability

Direct support testing procedures (performance tests) designed to check the serviceability of repaired items of equipment are included in section IV.

3-5. Correcting Trouble

The following information is included to aid in correcting equipment trouble that causes faulty operation.

a. Corrective measures are given in the troubleshooting charts.

b. The removal and replacement of parts is discussed in paragraph 3-29.

c. Instructions for performing transmitter adjustments when it is removed from the radio subsystem and connected to the test set are given in paragraph 3-28.

3-6. Troubleshooting Techniques

Effective troubleshooting must be systematic. Seldom is it possible to observe a symptom of trouble and immediately diagnose the cause. Usually, it will be necessary to perform a sequence of operational checks, observations, and measurements before the cause of a trouble is revealed. If the proper sequence is followed, the trouble will be traced first to a functional subgroup and then to a defective assembly, module, or printed circuit card. This sequence of steps is commonly referred to as sectionalization, localization, and isolation of trouble. The following is a list of six logical steps to follow in order to troubleshoot the equipment effectively and efficiently.

a. History of Equipment. The repairman can obtain helpful information by questioning organizational maintenance personnel, by reading the complaint notice attached to the equipment, and by reading the equipment log. The more information the repairman can gather, the more accurate his diagnosis will be and the sooner the trouble can be located and repairs made.

b. Preliminary Examination. A preliminary examination will help in gathering evidence that may lead to the location of the defect. Symptoms may be obtained through a quick check by observing the equipment for abnormal meter readings, lighted blown-fuse indicators, detecting the odor of burned insulation and parts; and by listening for high voltage arcing or other abnormal sounds that might indicate malfunctioning.

c. Sectionalization. Sectionalization of trouble consists of tracing the trouble to the functional subgroup responsible for the abnormal performance. The functional subgroups are modulation, signal control, frequency selection, frequency synthesizer, RF translator, and power supplies. Use the information obtained from the procedures given in *a* and *b* above and the abnormal indications portion of the troubleshooting chart as a quick check in sectionalizing the trouble. Perform each step (or applicable steps) in the troubleshooting chart to sectionalize the trouble to a particular functional subgroup if any of the following conditions exist:

(1) The observed symptoms in the quick check do not clearly indicate which particular functional subgroup is defective.

(2) The defect has caused the entire set or a major portion of the set to be inoperative.

(3) Troubleshooting of a particular functional subgroup has been attempted by using observed symptoms in the quick check, and the defect has not been found. Many abnormal indications can be caused by a defective part in one of several possible interrelated circuits. Procedures for sectionalizing to a particular functional subgroup are given in the troubleshooting chart.

d. Localization. Localization of trouble consists of tracing the trouble to the faulty assembly or plug-in printed circuit (PC) card. Localization is the final step in the direct and general support troubleshooting effort. After sectionalization has determined which functional subgroup has failed, perform the appropriate steps in the troubleshooting chart to locate the failed item.

e. Isolation. After the trouble has been localized, the next step is to isolate it to the defective part. Since component (transistor, resistor, etc.) replacement is not a direct support level function, the failed assembly or plug-in PC card should be forwarded with appropriate description of failure symptoms to the responsible maintenance facility for repair.

f. Testing After Repairs. After faulty parts are located and replaced, the equipment may not be free of faults. Some other fault (which has not been detected and corrected) may have caused the failure of the part that has been replaced, or the repairman may have inadvertently caused a trouble. After parts have been replaced, the equipment should be given an overall performance test (para 3-31) and the results compared with the performance requirements of the equipment.

3-7. Rack-Mounted and Bench Testing

Both rack-mounted performance tests (para 3-31) and bench performance tests (para 3-32) are provided at the general support maintenance level.

3-8. Transmitter Interchangeability

Nonrepairable transmitter failures may occur where no replacement transmitter is readily available. This requires the use of the other operable transmitter in order to restore the radio subsystem in use to normal operation. The primary No. 1 transmitter (6A9) and the secondary transmitter (6A11) are completely interchangeable with no modifications required.

3-9. Troubleshooting Data

a. General. In addition to the troubleshooting charts, other troubleshooting data is supplied to help the repairman rapidly locate trouble. The following types of troubleshooting data are supplied and should be consulted when necessary.

b. Voltage and Frequency Chart. A voltage and frequency chart (para 3-25) is provided for each replaceable assembly or module. This type of chart gives normal voltage and frequency measurements at key connector pins and at other significant points and is helpful when making voltage and/or frequency measurements to trace the fault to a specific part. When using the voltage and frequency chart, carefully read the notes and duplicate exactly the conditions under which the readings were obtained.

c. Waveform Illustrations. Waveform illustrations are provided (see para 3-26). These illustrations give normal waveforms at given key test points throughout the transmitter and are helpful in localizing the trouble to a specific PC card or module. When using these diagrams, carefully read the notes and duplicate exactly the conditions under which the waveforms were obtained.

d. Interconnection Diagrams. In general, the interconnection diagrams show the electrical interrelationship among the assemblies, subassemblies, and PC cards of the transmitter. By observing the symptoms with the use of the voltage and frequency table and analyzing their possible causes, it is often possible to trace the cause of faulty operation to a particular block on this diagram. The interconnection diagram for the transmitter is illustrated in figure FO-43.

e. Schematic Diagrams.

(1) A complete schematic diagram is provided for each assembly, subassembly, module, or PC card in the transmitter. This type of diagram shows all the circuitry and can be used as an aid in determining the faulty part in a particular component.

(2) Each PC card, subassembly, and module connector is identified by a block number (fig. FO-46); i.e., dual balanced modulator channel A1/B1 connector is J301, and dual balanced modulator channel A2/B2 connector is J303, etc. Table 3-1 lists the block number associated with each reference designation. Furthermore, the RF translator (A1) and the frequency synthesizer (A2) each have further block numbering breakdowns within each assembly. Table 3-1 also lists the block numbers with the associated reference designation of the circuits within each of these assemblies. In addition, all front panels and chassis-mounted piece parts are identified by block numbered reference designations, i.e. K302, CR303, R301, etc.

Table 3-1. Cross-Reference of Circuit Block Numbers to Reference Designations

Block number reference	Reference designation	Assembly, PC card, or module name
300	----------	Front panels and chassis.
301	A7	Dual balanced modulator Channel A1/B1.
302	A3	Channel A1/B1 filter pair.
303	A21	Dual balanced modulator Channel A2/B2.
304	A6	Channel A2/B2 filter pair.
305	A9	Multiplex carrier generator.
306	A5	Signal control
307	A4	Transmit gain control
308, 309, 310	A13, A14, A15	Frequency select memory.
311	A16	Band control
312	A17	Code conversion matrix No. 1
313	A18	Code conversion matrix No. 2
314	A8	Automatic channel loading
2000	A2A9	Master clock oscillator
2200	A2A1A1	5-MHz amplifier component board.
2100 and 2200	A2A2	Harmonic selector
2300	A2A2A2	Buffer amplifier
2400	A2A2A3	Video amplifier and mixer.
2500	A2A1	5-MHz amplifier
2600	A2A2A1	Logic control
2700	A2A3A3	In-lock indicator
2800	A2A6	RF box No. 2
2900	A2A6A1	Variable divider synthetic pump.
3000	A2A6A2	1-6-MHz phase-lock loop.
3100	A2A5	RF box No. 1
3200	A2A5A1	Master clock divider
3300	A2A5A2	Variable divider 2nd L.O.
3600 and 3700	A2A4	RF section 2nd L.O.
3700	A2A4A1	10 MHz VCXO
3700	A2A4A2	Differential amplifier
3800	A2	Frequency synthesizer
3800	A2A8	Filter box
5100	A1A2	Converter
5200	A1A3	Video amplifier
5300	A1A5	Low-pass filter

Block number reference	Reference designation	Assembly, PC card, or module name
5400	A1A4	Filter box
5400	A1	RF translator
5500	A1A6	−7-volt voltage regulator.
5800	A2A3	Hf VCO
6000	A2A3A2	Control loop
6100	A2A7	1-6-MHz VCO
6300	A2A3A1	Preset
6600	A1A1	Preamplifier
PS1	A19	−28 Vdc power supply
PS3	A10	+6.4 Vdc power supply
PS2	A11	+20 Vdc power supply

(3) Transmitter-schematics contain references to a numbered and/or lettered configuration. The numbered and/or lettered configuration as referenced on the schematic diagram relates to the dash number and/or letter following the assembly part number stenciled on the assembly.

Example: 233–00–638–1, the –1 represents the number configuration:
233–00–299–A, the –A represents the lettered configuration:
233–00–799–1A, the –1A represents the numbered and lettered configuration.

f. Parts Location Diagrams. The locations of transmitter assemblies replaced at direct support level are illustrated in figure FO–48.

g. Resistor, Capacitor, and Inductor Color Code Diagram. This diagram (fig. FO–1) is used to interpret the color codes used to indicate the values of resistors, capacitors, or inductors and their tolerances. Tolerance indicates the maximum difference in resistance, capacitance, or inductance that is expected between the rated value and the actual value of the resistor, capacitor, or inductance.

3–10. Waveform Analysis

a. Waveforms may be observed at various key test points in the transmitter. Oscilloscope AN USM–281 was utilized to record the waveforms illustrated in this manual. The time base used and the amplitudes of the waveforms are given with the waveforms so that other types of oscilloscopes can be readily used. The normal waveforms that should be obtained at key input/output test points and at other significant points are described (para 3–26). Before comparing the observed waveforms with the normal waveforms, carefully read the notes on the waveform illustrations and duplicate the conditions under which the normal waveforms were obtained.

b. A departure from the normal waveform indicates trouble between the point at which the waveform is observed to be normal and the point at which the waveform is observed to be abnormal. *For example,* if a waveform is observed to be normal at the input of a PC card and abnormal at the output of the same card, it is an indication that the trouble is in the card. When trouble is indicated, replace the faulty card or module before making any further tests. If replacing the card or module does not correct the trouble, take voltage and frequency measurements at the associated card or module connector pins (para 3–25).

3–11. Voltage and Frequency Measurements

Voltage and frequency measurements aid in determining circuit conditions and in evaluating clues in the course of troubleshooting. Compare the measured values of voltage and frequency with the normal values. If possible, use the same model test equipment with which the normal readings were obtained. Carefully read the notes on the diagrams and duplicate the conditions under which the normal readings were obtained. Dc voltages were measured using differential voltmeter ME–202/U, and ac voltages were measured using RMS voltmeter ME–30A/U. When making frequency measurements use frequency counter model AN/USM–207.

3–12. Blown Fuses

a. General. Fuses and blown-fuse indicators are located on the front panel of the transmitter. When a blown-fuse indicator is illuminated, it indicates a blown fuse. It is possible that the fuse has blown due to a momentary surge of current. By using the transmitter interconnection diagram (fig. FO–46) and following the direction given in *b* below, the trouble can be isolated.

b. Location of Trouble. When a blown-fuse indicator is illuminated, replace the fuse. If the replaced fuse indicator again illuminates, refer to the troubleshooting charts (para 3–23). Transmitter front panel blown-fuse indicator F301 (upper) illuminates when there has been an overload condition on the 120 Vac input line. Blown-fuse indicator F302 (lower) illuminates when there has been an overload condition in −28V power supply assembly (A19).

3–13. Reference Designation Number Location

a. General. Reference designations which are assigned to each part in the transmitter indicate the type of part and the location of the part. The transmitter employs the unit numbering system detailed below.

b. Unit Numbering System. In the unit numbering system, all parts in each major unit and all parts on the individual subassemblies within the unit are numbered consecutively beginning with 1 (*example:* J1, J2, S1, S2, etc.). The unit and subassemblies are then assigned prefix designations which are added to the part reference designation to indicate in which unit and what subassembly within the unit the part is located. *For example,* the transmitter units are designated 6A9 or 6A11 in the AN/TSC–38B system, (unit 6, subunit A9 or A11) and the frequency synthesizer assembly within each transmitter is designated A2 (thus, 6A9A2, 6A11A2). Within the synthesizer assembly there are nine individual subassemblies designated A1 through A9. One of these subassemblies is the hf VCO subassembly A2A3. Within the hf VCO subassembly there are three printed circuit cards designated A2A3A1, A2A3A2, and A2A3A3. One of these printed circuit cards is the in-lock indicator A2A3A3. Therefore, the complete reference designation for the in-lock indicator printed circuit card is 6A9A2A3A3 or 6A11A2A3A3. The complete reference designation for the transmitter POWER ON/OFF switch is 6A9S301 or 6A11S301.

c. Table Description. Table 3–2 lists the reference designations assigned to the assemblies, subassemblies, modules, printed circuit cards, and circuits that make up the transmitter. This table also provides a cross-reference index to applicable schematics and interconnection diagrams.

Table 3–2. Reference Designation Number Locations

Reference designation number	Unit, assembly, subassembly, module PC cards, and circuits	Figure No.
6A9, 6A11	Transmitter	FO–46
A1	RF translator	FO–48
A1A1	Preamplifier	2–8
A1A2	Converter	FO–12, FO–13
A1A3	Video amplifier	FO–15
A1A4	Filter box	2–10
A1A5	Low pass filter	FO–14
A1A6	−7-volt voltage regulator.	2–9
A2	Frequency synthesizer.	FO–47
A2A1	5-MHz amplifier	FO–28
A2A1A1	5-MHz amplifier component board.	FO–28
A2A2	Harmonic selector	FO–30
A2A2A1	Logic control	FO–33
A2A2A2	Buffer amplifier	FO–31
A2A2A3	Video amplifier and mixer.	FO–32
A2A3	Hf (pump) VCO assembly.	FO–24
A2A3A1	Preset	FO–26
A2A3A2	Control loop	FO–25
A2A3A3	In-lock indicator	FO–27
A2A4	2nd L.O. RF section	FO–38
A2A4A1	10 MHz VCXO	FO–38
A2A4A2	Differential amplifier	FO–38
A2A5	RF box No. 1	FO–41
A2A5A1	Master clock divider	FO–27
A2A5A2	2nd L.O. variable divider.	FO–40
A2A6	RF box No. 2	FO–42
A2A6A1	Variable divider synthesizer pump.	FO–35
A2A6A2	1–6-MHz phase-lock loop.	FO–36
A2A7	1–6 MHz VCO	FO–34
A2A8	Filter box	FO–43
A2A9	Master clock oscillator.	None
A3	Channel A1/B1 filter pair.	2–5
A4	Transmit gain control.	FO–9
A5	Signal control	FO–8
A6	Channel A2/B2 filter pair.	2–6
A7	Dual balanced modulator channel A1/B1.	FO–6
A8	Automatic channel loading.	FO–10
A9	Multiplex carrier generator.	2–7
A9A1	93.710-kHz oscillator	2–7
A9A2	106.29-kHz oscillator.	2–7
A10	+6.4 Vdc power supply.	FO–45
A11	+20 Vdc power supply.	FO–44
A12	41-pin extender card	None
A13, A14, A15	Frequency select memory.	FO–16
A16	Band control	FO–17
A17	Code conversion matrix No. 1.	FO–18
A17A1	100's of kHz	FO–18
A17A2	10's of kHz	FO–18
A18	Code conversion matrix No. 2.	FO–19
A18A1	Units of kHz	FO–19
A18A2	100's Hz	FO–19

Reference designation number	Unit, assembly, subassembly, module PC cards, and circuits	Figure No.
A19	−28 Vdc power supply.	2-12
A20	31-pin extender card	None
A21	Dual balanced modulator channel A2/B2.	FO-6

3-14. Replacing Parts

Careless replacement of parts often creates new troubles. When replacing parts, observe the following precautions.

a. Before a part is unsoldered, note the position of the leads. If a part, such as a transformer or a switch, has a number of connections tag each of the leads to make the proper connections when replacing the part. Be careful not to damage other leads by pulling or pushing them away. During soldering and unsoldering operations, dissipate excessive heat by holding the component lead with a pair of pliers.This is particularly important when the part concerned is a crystal diode.

b. Parts that require much time and effort for replacement should be checked thoroughly before removal to determine that the fault is within the suspected part and not in the associated circuitry.

c. After replacing an electrical component, check continuity before applying power. After replacing a mechanical part, manually check for proper freedom of motion before applying power.

d. It is very important to make well-soldered joints. A carelessly soldered joint may create a new trouble and it is one of the most difficult troubles to locate. Be careful not to allow drops of solder to fall into the equipment because they may cause short circuits.

e. When replacing a part in an RF circuit, place it in exactly the same position as the original part. A part which has the same electrical value but different physical size may cause trouble in high frequency circuits. In such a circuit, use the same type of capacitor for replacement and the same length because of the self-resonant frequencies of different brands of capacitors. When replacing parts in high frequency circuits, give particular attention to proper grounding; use the same ground used in the original wiring. Failure to observe these precautions when replacing parts in high frequency circuits may result in decreased gain or possibly unwanted conditions.

f. Whenever a part has been replaced, make any adjustments necessary and check the performance of the equipment to be sure that the original trouble has been remedied and that no new trouble has developed in the equipment.

g. Section III gives the general precautions and directions that apply to the removal and replacement of transmitter parts. Disassembly and reassembly of mechanically complicated assemblies is described where applicable.

3-15. Isolating by Parts Substitution

a. New plug-in components may be substituted for failure suspect components after trouble has been localized to a specific stage. When it is suspected that a capacitor is open, a known good capacitor of equal value may be connected across the suspected capacitor to check its operation. Parts must not be substituted indiscriminately, and a new component must not be left in a circuit in place of an original component if its presence in the circuit does not result in an improvement of the equipment performance. Replace components that must be unsoldered, or are diffcult to remove, only after the following conditions have been met:

(1) The trouble has been localized to a specific stage.

(2) Capacitors suspected of being open have been proved open by being bridged with known good capacitors.

(3) Voltage and resistance readings have been made and evaluated.

(4) Other suspected plug-in items have been replaced.

b. An example of types of defective components that may not be discovered by the procedures given in (1) through (4) above are an interstage transformer with a few shorted turns, and a capacitor that has changed value.

3-16. Intermittents

a. If the operation of a component is intermittently faulty, the trouble may be difficult to locate when the component is functioning normally. Such troubles can often be found by lightly taping each part in the suspected stage or portion of the component with a nonmetallic or insulated rod and, at the same time, watching the applic-

able meter. If the meter indication remains normal, repeat the tapping process at adjoining stages until the normal indications change.

b. Following is a list of faults which may cause intermittent operation:

(1) Defective controls.

(2) Loose connections.

(3) Poorly soldered joints.

(4) Cracked resistors.

(5) Defective semiconductors.

(6) Grit, lint, dust, or moisture between the plates of variable capacitors or inductors.

(7) Dirty, fractured, or imperfect insulators.

(8) Dirty or corroded fuse holders, transistor sockets, relay contacts or cable connectors.

(9) All parts, especially resistors, that may be cracked, blistered, bulged, charred, burned, or that contain other defects.

(10) Shock sensitive semiconductor components.

(11) Temperature sensitive semiconductor components.

3–17. Cable Checks

When checking cable conductors for continuity, it is very often inconvenient to bring the ends of the cable together, particularly when the cable is strapped in place, or runs through covered floor channels, or runs to a distant unit. In such cases, the ohmmeter leads are not always long enough to be connected to both ends of the cable. The procedure outlined in *a* through *h* below is given as a convenient method for checking for continuity or a short of single conductor and multiconductor cables when it is not practicable to bring the cable ends together.

a. Disconnnect both ends of the cable to be tested.

b. Select the first conductor in the cable (conductor labeled 1 or A, etc.) and ground it at one end.

c. Select the second conductor and connect an ohmmeter between the second conductor and the ungrounded end of the first conductor. The ohmmeter should indicate a reading of infinity. If a resistance value or a short circuit is indicated, then there is leakage or a short circuit between the two conductors. Locate and repair the fault.

d. If the ohmmeter indicates a normal reading of infinity, ground the other end of the second conductor. The ohmmeter should now indicate continuity.

e. If the ohmmeter still indicate infinity, one of the two conductors is open and a higher category of maintenance is required for cable repair.

f. Leave the second conductor grounded at one end and disconnect the ohmmeter from the other end.

g. Select the third conductor and repeat the methods as outlined in steps *c* through *f* above.

h. Follow the same procedure for the remaining conductors in the cable. When the check is completed, disconnect all grounded conductors.

3–18. Tools and Test Equipment

Special tools (table 3–3) and test equipment (table 3–4) required for direct support maintenance as authorized by the maintenance allocation chart (MAC). Equivalent instruments may be used unless otherwise stated. The information provided in these tables is not to be used as a basis for requisitioning.

3–19. Parts Location Diagrams

The location of each transmitter (6A9 and 6A11) in its normal system configuration is illustrated in TM 11–5895–356–12–1. Transmitter assemblies and parts locations are illustrated in figure FO–48.

Section II. TROUBLESHOOTING AT DIRECT SUPPORT

3–20. General

This section provides troubleshooting data at the direct support maintenance level for the transmitter. The troubleshooting data consists of troubleshooting charts, voltage and frequency measurements, and troubleshooting waveforms. Troubleshooting the transmitter consists of testing the unit at various levels to determine where the malfunction has occurred, and then either performing readjustment or replacement of the defective assembly or module.

Table 3-3. Special Tools for Direct Support

Quantity	Description
1 each	Printed circuit card extractor—supplied with unit.
1 each	31-pin printed circuit card extender—supplied with unit.
1 each	41-pin printed circuit card extender—supplied with unit.
1 each	Power supply load resistor 25Ω 100W wirewound tapped at 3.7Ω for +6.4 V load and 10.5Ω for +20 V load—not supplied with unit.
1 each*	RF translator extender cable—not supplied with unit.
1 each*	Synthesizer extender cable—not supplied with unit.
7 each*	RF extender cables—not supplied with unit
1 each**	Synthesizer printed circuit card extender—not supplied with unit.

*RF translator extender cable consists of Cannon connectors DCM-9P and DCM-9S wired pin-to-pin with 24 inches of AWG #24 standard wire.
Synthesizer extender cable consists of Cannon connectors DCM-50P and DCM-50S wired pin-to-pin with 24 inches of AWG #24 standard wire.
RF extender cables consist of Selectro connectors 51-027-0000 and 51-024-0000 using 24 inches of RG-188 A/U cable.
**Synthesizer printed circuit card extender can be supplied upon request (part number 233-00-036).

b. Trouble analysis is first performed with the transmitter mounted in the rack (unit 6) using the rack-mounted troubleshooting chart 3-1. The rack-mounted troubleshooting chart is provided to insure that the transmitter is not indiscriminately removed from the rack before all practical in-rack troubleshooting efforts are exhausted. The rack-mounted troubleshooting chart is designed to enable the repairman to locate trouble based on indications obtained while the transmitter is functioning as part of the radio subsystem. Reference is made to the bench troubleshooting chart when further troubleshooting in the rack is not practical.

c. Bench trouble analysis may be performed when frequency synthesizer adjustments are necessary or when more detailed troubleshooting efforts are required. The bench troubleshooting chart 3-2 is designed to enable the repairman to locate trouble based on indications obtained while the transmitter is removed from the radio subsystem and connected to the receiver-transmitter test set (T324732A).

Table 3-4. Direct Support Maintenance Test Equipment

Nomenclature	Federal stock No.	Common name
AN/USM-207 Counter Electronic, Digital Readout	6625-911-6368	Frequency counter
AN/USM-210 Multimeter	6625-019-0815	VOM
ME-30A/U Voltmeter	6625-643-1670	RMS voltmeter
AN/URM-145 Voltmeter, Electronic	6625-973-3986	RF voltmeter
SG-479/GRM-50 Generator, Signal	6625-819-0472	Hf signal generator
AN/USM-281 Oscilloscope	6625-053-3112	
CN-796/U Attenuator, Variable	5985-087-2547	
AN/URM-127 Generator, Signal	6625-793-5964	Audio oscillator
8491A HP Attenuator, Fixed 20 db		
P6161 Stancor Transformer, Isolation		
T324732A Receiver Transmitter Test Set		Test set
CN-16A/U Transformer	5950-235-2086	Variac
PP-2309/U Power Supply (2)	6130-752-2215	
ME-303/U Multimeter	6625-902-7140	VTVM
ME-202/U Voltmeter, Differential	6625-709-0288	Fluke meter
Boonton 91-8B 50-ohm adapter probe		

3-21. Reference Data

The following data listed below will be helpful when using the troubleshooting charts:

Reference	Data
Table 3-2	Reference Designation, Schematics, Interconnection Diagrams, and Parts Location Diagrams.
Table 3-7	Voltage and Frequency Measurements
Figure 3-3	Transmitter Troubleshooting Waveforms Guide.
Figure 3-4	Transmitter Troubleshooting Waveforms
Table 3-8	Band Control Card A16 Signal Inputs
Table 3-9	Band Control Card A16 Signal Outputs
Table 3-10	Code Conversion Matrix Cards A17 and A18 Signal Outputs and Inputs.

3-22. Physical Test and Inspection

a. General. This procedure is provided for use as either the first step in troubleshooting, or use after repairs are completed and before the equipment is returned to the using organization.

b. Procedure.

WARNING

To prevent injury to personnel, disconnect ac-input power to transmitter before performing this procedure.

(1) Inspect front panel for evidence of physical damage, loose or missing parts.

(2) Inspect connectors and plugs for cleanliness and evidence of physical damage.

(3) Check all fuses for proper size and amperage rating.

(4) Check all filter capacitors for evidence of leakage or overheating.

(5) Check all resistors for evidence of discoloration due to overheating.

(6) Inspect all wiring and cabling for worn or frayed insulation, and broken, loose, or disconnected wires or cables.

(7) Inspect all metal surfaces, intended to be painted, for condition of finish and legibility of panel lettering.

NOTE

Touchup paint is recommended instead of refinishing whenever practical.

(8) Check the equipment for applicable modification work orders (MWO's).

(9) Inspect condition of moisture/fungus proofing.

(10) Inspect chassis for evidence of sprung or damaged frames, resulting in improper operation of interlocks when chassis is mounted into rack.

(11) Inspect overall unit for presence of dirt, corrosion, moisture, and bits of wire and solder inside the equipment.

3–23. Use of Troubleshooting Charts

a. The troubleshooting charts 3–1 and 3–2 provide a systematic step-by-step method of troubleshooting designed to diagnose the cause of trouble in the transmitter. Following the proper sequence of operational checks, observations, and measurements, trouble is traced through the normal steps of sectionalization, localization, and isolation to the defective assembly, plug-in module, or printed circuit card.

b. The step and procedure columns of the troubleshooting charts provide a sequence of test setup instructions and operational checks. The normal indication column gives the expected observations for comparison with the abnormal indication column to provide a failure symptom. More than one abnormal indication may be given for each normal indication. The corrective measures column provides a complete set of troubleshooting instructions for each abnormal indication. Furthermore, the corrective measures column reference applicable paragraph numbers where adjustments, repair, or further troubleshooting is required. In addition, reference is made to a higher category of maintenance if required for further troubleshooting.

c. Some normal indications are provided for operator convenience only and are therefore not associated with failures within the transmitter. In these cases, abnormal indications are not applicable and are therefore not provided. When similar procedural steps are repeated and have been previously troubleshot, abnormal indications and corrective measures are not repeated.

3–24. Troubleshooting Test Conditions

a. Rack-Mounted Troubleshooting. Initial power turn-on procedures and control settings are included and therefore, no initial test setup instructions are required. Test equipment connections are shown in figure 3–1.

CAUTION

To prevent permanent damage to the transmitter, insure that a 20-db fixed attenuator is connected to the RF patch panel (6A6) PRIM EXCITER/SEC EXCITER jack.

CAUTION

Testing is accomplished using the transmitter only. Insure that the two linear power amplifiers (unit 2, and unit 6A8) are deenergized by placing the following switches in the indicated positions:

Unit	*Switch*	*Position*
1A3	PRI LIN PWR AMP	down
1A2	SEC LIN PA	down
6A8	PRIMARY POWER ON/OFF	OFF
2	FIL ON/OFF	OFF
2	HV ON/OFF	OFF

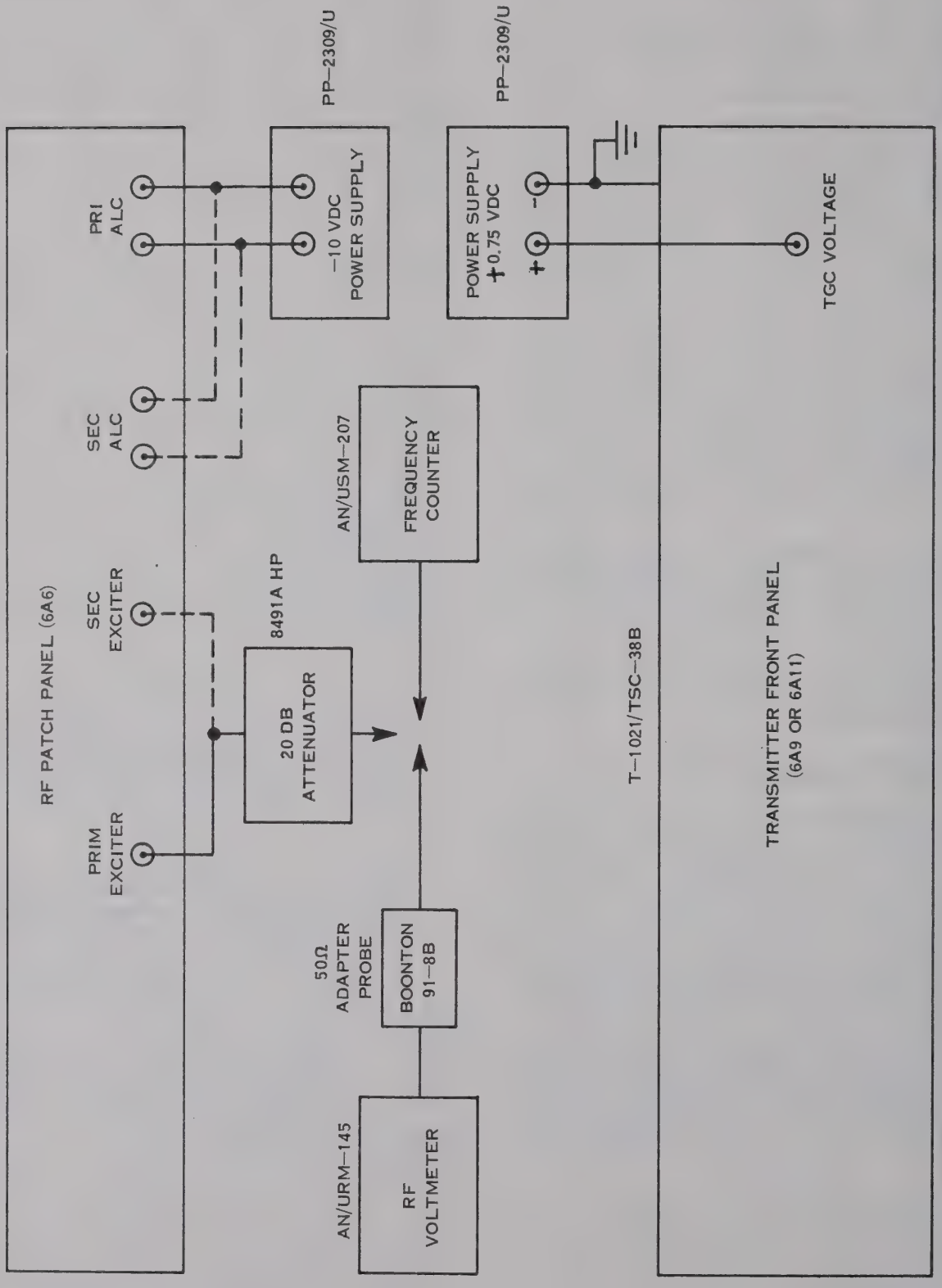


Figure 3-1. Rack-mounted test setup diagram.

Chart 3–1. Rack-mounted Troubleshooting Chart

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
1	Remove transmitter from rack, remove top and bottom covers, and reinstall unit into rack (para 3–29*a*). Energize radio subsystem in accordance with TM 11–5895–356–12–1, except for 10 kw P.A. (unit 2) or 1 kw P.A. (unit 6A8) linear power amplifiers. Set the transmitter 6A9 or 6A11) controls as listed below:			*Warning:* Voltages capable of causing injury or death may be present on J4, K301, fuses and power supply terminals.
	a. Set the EXCITER GAIN control to 10.			
	b. Set the CARRIER ADJUST–LOCAL switch to REMOTE.			
	c. Set the CARRIER ADJUST–LOCAL–STEP (−db) switch to 0.			
	d. Set the TGC ON/OFF switch to OFF (right) (table 3–12).			
	e. Set the ALC ON/OFF switch to ON (left) (table 3–12).			
	f. Apply +0.75 ±0.05 Vdc to the TGC VOLTAGE jack (fig. 3–1).			
	g. Set the transmitter POWER ON/OFF switch to ON.	*a.* POWER indicator (DS301) illuminates.	POWER indicator (DS301) fails to illuminate.	Remove upper fuse indicator (F301) and remove fuse. Reinstall fuse indicator and observe if indicator illuminates to indicate presence of ac power. If ac power is present, reinstall fuse (F301) and replace lamp (DS301); if ac power is not present, refer to bench troubleshooting para 3–24*b* and chart 3–2.
		b. Upper fuse indicator (F301) not illuminated.	Upper fuse indicator (F301) illuminated.	Replace blown fuse. Fuse indicator should not illuminate. If fuse indicator illuminates, refer to bench troubleshooting chart (para 3–24*b*).
		c. Lower fuse indicator (F302) not illuminated.	Lower fuse indicator (F302) illuminated.	Replace blown fuse. Fuse indicator should not illuminate. If fuse indicator does not illuminate, proceed to step 2; if fuse indicator illuminates, refer to bench troubleshooting para 3–24*b* and chart 3–2.

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
	Dc Voltage Checks			
	Caution: Insure transmitter power is off before removing or replacing modules.			
2	Using a card extraction tool remove signal control A5 PC card, insert 31-pin extender card A20 into J306 connector, and reinstall signal control A5 PC card (para 3–29*b*).			
	Using a differential voltmeter measure dc voltage at J306 pin A.	+20 ±0.1 Vdc	*a.* Voltage out of tolerance	Adjust +20 Vdc power supply A11 output voltage (para 3–28*b*).
			b. No output voltage	Higher category maintenance is required.
3	Using a differential voltmeter measure dc voltage at J306 pin H.	−20 ±0.1 Vdc	*a.* Voltage out of tolerance	Adjust −20 Vdc power supply circuit on the signal control PC card A5 (para 3–28*c*).
			b. No output voltage	Replace signal control PC card A5 (para 3–29*b*) and measure output voltage for −20 Vdc. If −20 Vdc is present, proceed to step 4; if −20 Vdc is not present, check for −25 to −38 Vdc on J306 pin C. If −28 Vdc is present, refer to bench troubleshooting chart (para 3–24*b*); if −28 Vdc is not present, higher category maintenance is required.
4	Using a differential voltmeter measure dc voltage at J306 pin B.	+6.4 ±0.05 Vdc	*a.* Voltage out of tolerance	Adjust +6.4 Vdc power supply (A10) output voltage (para 3–28*a*).
			b. No output voltage	Higher category maintenance is required.
	System Tuning Check:			
5	At the frequency select panel (7A4/7A11) select 29.9990 MHz on the TRANSMITTER FREQUENCY SELECT MEGACYCLES thumbwheel switches.			
	At the mode and status panel (7A5/7A12) set PWR ON pushbutton to ON, KEY LINE switch to XMIT, XMTR PLT CARR switch to VAR, and SIMPLEX switch to OFF. (pushbutton lamp extinguished). On the frequency select panel (7A4/7A11) depress the XMTR TUNE	SYS TUNING indicator on mode and status panel (7A5/7A12) illuminates for less than 5 seconds; then the KEYED indicator illuminates.	*a.* SYS TUNING indicator remains illuminated and KEYED indicator fails to illuminate. *b.* SYS TUNING indicator fails to illuminate.	Proceed to corrective measure in step 7. *a.* Systematically replace the following: (1) SYS TUNING indicator lamp. (2) TGC PC card A4 (para 3–29*b*).

	pushbutton.			(3) Frequency synthesizer (A2) assembly (para 3–29*d*). *b.* If step *a* fails to correct problem refer to bench troubleshooting chart.
6	*Rf Carrier Checks:* At the mode and status panel (7A5/7A12) set NORMAL LEVEL SEL switch to EXCITER RF. Adjust XMTR PLT CARR–VAR control for an RF output indication on the NORMAL LEVELS meter at the junction of green and red scales.	NORMAL LEVELS meter indicates at the junction between green and red areas.	NOMRAL LEVELS meter indicates no output (loss of transmitter RF output).	*a.* Connect the 50-ohm adapter probe of the RF voltmeter to the 20-db attenuator connected to PRIM EXCITER/SEC EXCITER jack on the RF patch panel 6A6 (fig. 3–1). A 0.45 ±0.05 Vrms level should be present on the RF voltmeter. *Note.* If voltage is out of tolerance, check NORMAL LEVELS meter calibration procedure in the system manual (TM 11–5895–356–34–1/1). (1) If step *a* above is not correct, connect the 50-ohm RF voltmeter probe to P5402 (RF input, fig. FO–2). A 100-kHz signal of 25 to 60 mv rms amplitude should be present. (a) If voltage level is correct at P5402 and NORMAL LEVEL meter indicates no output, replace RF translator A1 assembly (para 3–29*c*). (b) If voltage level is not correct at P5402, replace the signal control A5 PC card (para 3–29*b*). If replacement of signal control card fails to correct problem, replace frequency synthesizer (A2) assembly (para 3–29*d*). *b.* If procedures in step *a* fail to correct problem, refer to bench troubleshooting chart.
7	*Transmitter Frequency Checks:* On RF patch panel (6A6) connect frequency counter to 20-db attenuator at PRIM EXCITER/SEC EXCITER jack (fig. 3–1). At the frequency select panel (7A4/7A11) select any frequency from 2.0000 to	TRANSMITTER-READY and KEYED indicators on the mode and status panel (7A5/7A12) are illuminated following SYS TUNING indicator extinguishing. Counter should indicate a	SYS TUNING indicator remains illuminated and/or transmitter output frequency is incorrect.	*a.* Connect a frequency counter to the RF translator (A1) assembly connector P5403. Depress XMTR TUNE pushbutton on frequency select panel (7A4/7A11) for each frequency selected. Using

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
	29.9999 MHz on TRANSMITTER FREQUENCY SELECT MEGACYCLES thumbwheel switch. Depress XMTR TUNE pushbutton; insure that XMTR PLT CARR switch is set to VAR and SIMPLEX switch is set to off (pushbutton lamp extinguishes).	frequency within ±3 Hz of the frequency selected with the thumbwheel switches.		the TRANSMITTER FREQUENCY SELECT thumbwheel switches on the frequency select panel (7A4/7A11), select the frequencies listed in table 3–5. Frequencies observed at P5403 should be within tolerances specified in table 3–5. *Note.* If the counter reading is stable but the frequency is in error (and the error is consistently related to a given decade step), the fault is probably within one of the frequency select memory, band control, or code conversion matrix PC cards associated with the digit involved (see note in table 3–6). (1) Install a known-good card in place of the suspected card, using the 31-pin extender board. (2) If module replacement does not solve the problem, replace frequency synthesizer (para 3–29*d*). (3) If the above step fails to correct problem, refer to bench troubleshooting chart.
				b. Connect a frequency counter to the RF translator (A1) assembly connector P5404. Depress XMTR TUNE pushbutton on the frequency select panel (7A4/7A11) for each frequency selected. Using the TRANSMITTER FREQUENCY SELECT thumbwheel switch on the frequency select panel (7A4/7A11), select the frequencies listed in table 3–6. Frequencies observed at P5404 should be within tolerances specified in table 3–6. If frequencies are out of tolerance, replace frequency synthesizer (para 3–29*d*).

	TGC Function Check:			
8	Remove +0.75 Vdc from TGC VOLTAGE jack at transmitter front panel (fig. 3–1), and set TGC switch to ON (table 3–12). Connect RF voltmeter to 20-db attenuator at PRIM EXCITER/SEC EXCITER jack on RF patch panel (6A6) (fig. 3–1).	NORMAL LEVELS meter on the mode and status panel (7A5/7A12) should continuously sweep from orange to green area and reset. RF voltmeter should indicate at least 18-db change in level.	*a.* NORMAL LEVELS meter fails to scan. *b.* Scanning range is out of tolerance.	Replace TGC PC card A4 (para 3–29*b*). If replacement of TGC card fails to correct problem refer to bench troubleshooting. *a.* Replace signal control PC card A5 (para 3–29*b*). *b.* Apply an external −7 ±0.1 Vdc to TGC test jacks on RF patch panel 6A6 (fig. 3–1), and align TGC card (para 3–28*e*).
	Modulation Checks:			
9	At the mode and status panel (7A5/7A12) set KEY LINE switch to XMIT, XMTR PLT CARR switch to OFF, NORMAL LEVEL SEL switch to EXCITER AUDIO, and the NORMAL LEVEL, AUDIO SEL switch to position B2. Apply +0.75 Vdc to TGC VOLTAGE test point on transmitter front panel (6A9/6A11). Connect an RF voltmeter to 20-db attenuator at PRIM EXCITER/SEC EXCITER jack on RF patch panel 6A6 (fig. 3–1). Proceed as follows: *a.* Connect an audio oscillator to unit 7A15 patch panel. Apply a −6 dbm 1-kHz audio signal to PRIMARY/SECONDARY SEND B2 jack. Depress XMTR CH B2 switch to the on position (illuminated). Adjust MODULATION LEVEL B2 control on transmitter front panel for rated output power (0.45 Vrms at RF voltmeter). *b.* Set CH B2 switch to OFF position. Set AUDIO SEL switch to CH B1 and connect audio osc to unit 7A15 PRIMARY/SECONDARY SEND B1 jack. Repeat step 9*a*. *c.* Set CH B1 switch to OFF. Set AUDIO SEL switch to CH A1 and connect audio osc to unit 7A15 PRIMARY/SECONDARY SEND A1 jack. Repeat step 9*a*. *d.* Set CH A1 switch to OFF. Set AUDIO SEL switch to CH A2 and	NORMAL LEVELS meter on unit 7A5/7A12 indicates at approximate junction of orange and green region with NORMAL LEVEL SEL switch set to EXCITER AUDIO and STATUS TRANSMITTER lamps and CH B2, CH B1, CH A1 and CH A2 enabled individually. RF voltmeter should indicate a voltage level of 0.45 ±0.05 Vrms for each channel enabled.	*a.* NORMAL LEVELS meter indicates significantly above or below green level. *b.* RF voltmeter indication out of tolerance.	Check NORMAL LEVELS meter calibration procedure in the system manual (TM 11–5895–356–34/1/1). *a.* Systematically replace the following: (1) Signal control PC card A5 (para 3–29*b*). *Note.* If replacement of signal control PC card A5 corrects the problem, the original card may require alignment (para 3–28*g* and *h*). (2) ACL PC card A8 (para 3–29*b*). (3) Refer to the table below for PC cards applicable to a particular channel failure, and replace those cards in the order shown (para 3–29*b*). *CH A1* A3, A7, A2* *CH B1* A3, A7, A2* *CH A2* A6, A21, A9 *CH B2* A6, A21, A9 *Frequency synthesizer (para 3–29*d*). *b.* If procedures in step *a* above fail to correct problem, refer to bench troubleshooting.

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
	connect audio osc to unit 7A15 PRIMARY/SECONDARY SEND A2 jack. Repeat step 9*a*.			
	ALC Check			
10	On the transmitter front panel (fig. 1–1) adjust MODULATION LEVEL −A2 control for a level of 0.45 VRMS on RF voltmeter. Ensure that ALC ON/OFF switch (table 3–12) is set to ON (left position). Apply an external −10 +0.1 Vdc level to ALC test jacks on rf patch panel 6A6 (fig. 3–1). *Note:* Observe test jack polarity as shown in figure 3–1.	RF voltmeter level should decrease 22 ±2 db.	RF voltmeter level out of tolerance.	Replace signal control PC card A5 (para 3–29*b*). If replacement of signal control PC card fails to correct problem, higher category maintenance is required.
	AM Check:			
11	Set the STATUS TRANSMITTER–CH A2 switch on the mode and status panel (7A5/7A12) to off. On the transmitter front panel, set the CARRIER ADJUST–LOCAL switch to AM (fig. 1–1).	RF voltmeter should indicate 225 ±20 mv/rms.	RF voltmeter level out of tolerance.	Replace signal control PC card A5 (para 3–29*b*). If replacement of signal control PC card fails to correct problem, higher category maintenance is required.
	Tune Power Check:			
12	Place signal control PC card A5 on 31-pin extender card. Connect a jumper lead from J306 pin J to chassis ground.	RF voltmeter should indicate 0.2 ±0.05 Vrms.	RF voltmeter level out of tolerance.	Adjust R14 on ACL PC card A8 and/or R71 on signal control PC card A5 for correct level. If the above adjustment fails to correct problem, higher category maintenance is required.
13	Remove ground jumper and reinstall PC card A5 into chassis.			

b. Bench Troubleshooting. This test is to be performed with the transmitter on the bench, the transmitter front panel POWER ON/OFF switch initially set to OFF, and the top and bottom cover plates of the transmitter removed.

NOTE

Before connecting the test set to the transmitter in the next step, insure that the test set power is off.

CAUTION

To prevent permanent damage to the RF translator (A1) assembly output transistor, insure that a 50-ohm termination (20-db fixed attenuator) is connected to the transmitter output connector J1.

(1) Connect the test setup as shown in figure 3-2.

Table 3-5. Frequency Synthesizer A2 Pump Frequency Checks

Output pump (P5403)	Selected frequency MHz	Pump frequency at P5403
Digit Checks 1 kHz-10 MHz. (See note at table 3-6).	2.0000	88.9990 ±3 Hz
	2.1110	88.8880 ±3 Hz
	3.2220	87.7770 ±3 Hz
	4.3330	86.6660 ±3 Hz
	5.4440	85.5550 ±3 Hz
	6.5550	84.4440 ±3 Hz
	7.6660	83.3330 ±3 Hz
	8.7770	82.2220 ±3 Hz
	9.8880	81.1110 ±3 Hz
	10.9990	80.0000 ±3 Hz
	21.0000	69.9990 ±3 Hz
1-6-MHz VCO Band Checks. (See note at table 3-6).	2.0000	88.9990 ±3 Hz
	2.1990	88.8000 ±3 Hz
	2.2000	88.7990 ±3 Hz
	2.4990	88.5000 ±3 Hz
	2.5000	88.4990 ±3 Hz
	2.8990	88.1000 ±3 Hz
	2.9000	88.0990 ±3 Hz
	2.9990	88.0000 ±3 Hz
	3.0000	87.9990 ±3 Hz
	3.3990	87.6000 ±3 Hz
	3.4000	87.5990 ±3 Hz
	3.9990	87.0000 ±3 Hz
	4.0000	86.9990 ±3 Hz
	4.7990	86.2000 ±3 Hz
	4.8000	86.1990 ±3 Hz
	4.9990	86.0000 ±3 Hz
	5.0000	85.9990 ±3 Hz
	5.7990	85.2000 ±3 Hz
	5.8000	85.1990 ±3 Hz
	6.9990	84.0000 ±3 Hz
Hf VCO Band edge checks		
Band 1	2.0000	88.9990
	6.9990	84.0000
2	7.0000	83.9990
2	11.9990	79.0000
3	12.0000	78.9990
3	16.9990	74.0000
4	17.0000	73.9990
4	21.9990	69.0000
5	22.0000	68.9990
5	26.9990	64.0000
6	27.0000	63.9990
6	29.9990	61.0000

Table 3-6. Frequency Synthesizer A2 L.O. Frequency Digit Checks

L.O. Output (P5404)	Selected frequency MHz	2nd L.O. Frequency MHz at P5404
Hundreds-of-Hz Checks. (See note).	2.0000	90.8990
	2.0001	90.8991
	2.0002	90.8992
	2.0003	90.8993
	2.0004	90.8994
	2.0005	90.8995
	2.0006	90.8996
	2.0007	90.8997
	2.0008	90.8998
	2.0009	90.8999

NOTE

Each frequency increment from hundreds-of-Hz to tens-of-MHz is associated with two plug-in (PC) cards. The following lists each frequency increment and the PC card associated with the increment.

Frequency increment	*Card*
Tens-of-MHz and units-of-MHz.	Frequency select memory No. 1 (A13) or band control (A16).
Hundreds-of-kHz and tens-of-kHz.	Frequency select memory No. 2 (A14) or code conversion matrix No. 1 (A17).
Units-of-kHz and hundreds-of-Hz.	Frequency select memory No. 3 (A15) or code conversion matrix No. 2 (A18).

(2) Set the test set (T324732A) controls as listed below:

Control/Indicator	*Setting*
PWR-SET switch	SET (up position)
PWR indicator	illuminated
PWR-XMTR switch	XMTR (up position)
PC switch	down position (off)
KEY switch	up position (on)
TUNE PWR switch	down position (off)

Control/Indicator	*Setting*
AUDIO INPUT CH A1	down position (off)
CH A2	down position (off)
AUDIO INPUT CH B1	down position (off)
CH B2	down position (off)
PC-LVL control	midrange
FREQUENCY SELECT switch.	set to 02.5000 MHz
OSC-LVL control	midrange
OSC select switch	OFF

(3) Set the transmitter controls as listed below:

Control/Indicator	*Setting*
EXCITER GAIN control	10
CARRIER ADJUST-LOCAL switch.	REMOTE
CARRIER ADJUST-LOCAL-STEP (-db) switch.	0
TGC ON/OFF switch	OFF (fig. FO-51)
ALC ON/OFF switch	ON (fig. FO-51)
TGC VOLTAGE jack	Apply +0.75 ±0.05 Vdc
POWER ON/OFF switch	ON

NOTE

XMTR DTE indicator on test set illuminates for 5 seconds or less when the transmitter POWER ON/OFF switch is set to the ON position.

(4) Using a differential voltmeter, measure transmitter power supply voltages, −20 Vdc, +20 Vdc and ±6.4 Vdc on signal control PC card A5. See table 3-7, signal control PC card A5, for pin numbers and the voltage tolerances.

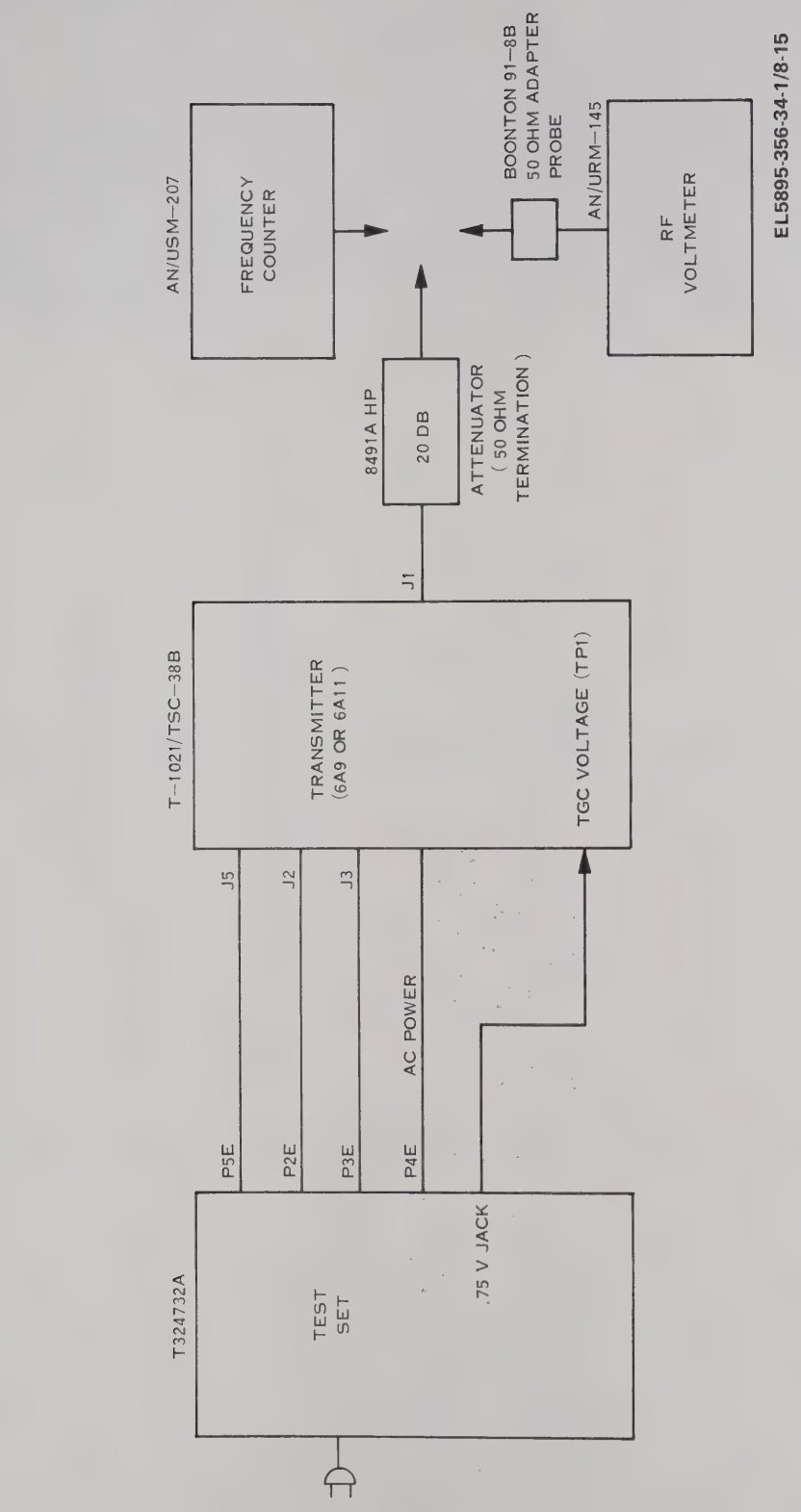


Figure 3-2. Transmitter bench test setup diagram.

Chart 3-2. Bench Troubleshooting Chart

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
	Warning: Voltages capable of causing injury or death may be present on J4, K301, fuses, and power supply terminals.			
1	Refer to paragraph 3-24*b* for transmitter bench setup and power turn-on procedures.	*a.* POWER indicator (DS301) illuminates.	POWER indicator (DS301) fails to illuminate.	Remove fuse indicator F301 (upper) and remove fuse. Reinstall fuse indicator and observe that fuse indicator illuminates to indicate the presence of ac power. *a.* If ac power is present, reinstall fuse F301 and replace lamp DS-301. *b.* If ac power is not present, reinstall fuse F301. Set test-set PWR switch to off and on and observe relay K301 actuating. (1) If relay K301 actuates, place VOM ac probes on K301 pin 9 and chassis ground; 120 Vac should be observed. If 120 Vac is present, higher category maintenance is required. If 120 Vac is not present, replace relay K301. (2) If relay K301 does not actuate place positive dc probe of VOM on K301 pin 1 and negative probe on chassis ground. If +28 Vdc is present, replace relay K301. If +28 Vdc is not present, higher category maintenance is required.
		b. Fuse indicator F301 (upper) not illuminated.	Fuse indicator F301 (upper) illuminated.	Replace blown fuse; fuse indicator should not illuminate. If fuse indicator does not illuminate, proceed to step 2. If fuse indicator illuminates, higher category maintenance is required.
		c. Fuse indicator F302 (lower) not illuminated.	Fuse indicator F302 (lower) illuminated.	Replace blown fuse; fuse indicator should not illuminate. If fuse indicator does not illuminate, proceed to step 2. If fuse indicator illuminates, disconnect P3801 from synthesizer (A2), P5405, from RF translator (A1), and remove

				transmit gain control PC card A4. Replace blown fuse; fuse indicator should not illuminate. *a.* If fuse indicator does not illuminate, reconnect each assembly one at a time until fuse indicator illuminates; then replace failed assembly and fuse. *b.* If fuse indicator illuminates higher category maintenance is required.
	Dc Voltage Checks: **Caution:** Insure receiver power is off before removing or replacing modules.			
2	Set transmit gain control A4 PC card on 31 pin extender card A20 (para 3–29*b*). Using a differential voltmeter, measure dc voltage at J307 pin A.	+20 ±0.1 Vdc	*a.* Voltage out of tolerance	Adjust +20 Vdc power supply A11 output voltage (para 3–28*b*).
			b. No output voltage	Higher category maintenance is required.
3	Using a differential volmeter, measure dc voltage at J307 pin *k*.	−20 ±0.1 Vdc	*a.* Voltage out of tolerance	Adjust −20 Vdc power supply circuit on the signal control PC card A5 (para 3–28*c*).
			b. No output voltage	Replace signal control PC card A5 (para 3–29*b*) and remeasure output voltage. If −20 Vdc is present, proceed to step 4. If −20 Vdc is not present, check for −28 Vdc on J306 pin C. *a.* If −28 Vdc is present, remove the transmit gain control A4 PC card, automatic channel loading A8 PC card, and synthesizer A2 cable P3801. Systematically reinstall each cable and assembly until defective module is isolated. Replace defective module. *b.* If −28 Vdc is not present, higher category maintenance is required.
4	Using a differential voltmeter, measure dc voltage at J307 pin B.	+6.4 ±0.05 Vdc	*a.* Voltage out of tolerance	Adjust +6.4 Vdc power supply A10 output voltage (para 3–28*a*).
			b. No output voltage	Higher category maintenance is required.
	System Tuning Check:			
5	At the test set (T324732A) select	XMTR DTE indicator lamp on	XMTR DTE indicator lamp re-	*a.* Connect a test cable with a 1X

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
	29.9990 MHz on the FREQUENCY SELECT thumbwheel switches and depress the XMTR DTE pushbutton.	test set illuminates for less than 5 seconds.	mains illuminated and transmitter does not tune.	probe between the vertical INPUT of a test oscilloscope and test point TP8 on transmit gain control card A4 (fig. FO–51). Set oscilloscope as follows: Triggering ..... MAIN INT SWEEP MODE ... NORM MAGNIFIER ..... X1 TIME/DIV ..... 10MS/CM VOLTS/DIV ..... 2 *b.* Depress the XMTR DTE pushbutton on the test set while observing the oscilloscope. A momentary 40-ms pulse at +4 ±0.5-V amplitude should be observed. *c.* If a 40-ms pulse is not present, measure the input to the TGC card A4 between J307 pin P and ground with a multimeter set to dc volts. Depress the XMTR DTE pushbutton on the test set; 0 Vdc level should be observed. If the 0 Vdc level is not obtained, higher category maintenance is required. *d.* If the 0 Vdc level is correct and the 40-ms pulse is not present, replace transmit gain control card A4 (para 3–29*b*). *e.* If the 40-ms pulse is correct and the 0 Vdc level is present and replacement of A4 does not correct the failure, continue to steps 6 and 7.
	RF Carrier Checks:			
6	Connect the test set +0.75V jack to the TGC VOLTAGE test jack on the transmitter front panel. Connect the 50-ohm terminated probe of the RF voltmeter to the 20-db attenuator (fig. 3–2). At the test set, set KEY switch to up position and PC switch to up position.	A 0.45V rms or greater level should be present on the RF voltmeter.	Voltage out of tolerance	*a.* At the test set, set the KEY switch to the down position and connect the 20-db attenuator (fig. 3–2) to J5401 (fig. FO–46) using a BNC/TNC Sealectro adapter. Set KEY switch to the up position; 0.45 Vrms or greater level should be indicated. If voltage is correct, reconnect coaxial cable P5401 to J5401.

b. If the 0.45V or greater level is not correct, connect the 50-ohm RF voltmeter probe to P5402 (RF input) at RF translator (A1). A 100-kHz signal of 25 to 60 mv amplitude should be present. Connect a test cable between P5403 at RF translator (pump) and the digital electronic counter plug-in unit INPUT jack. Set counter controls as follows:

INPUT	PLUG-IN
TIME BASE	1 SEC
FUNCTION	FREQ
FREQ. DIAL	60

A frequency readout of 1000.000 kHz ±3 Hz which corresponds to 61 MHz should be observed; record this indication. Move the test cable from P5403 at RF translator A1 to P5404. Set counter FREQ DIAL to 90. A 899.000-kHz ±3 Hz readout corresponding to 90.899 MHz should be indicated; record this indication. If the signals of P5403, and/or P5404 are incorrect proceed to step 7. If signals at P5402, P5403 and P5404 are correct and the 0.45 Vrms signal is incorrect, replace RF translator module A1 (para 3–29*c*). If replacement of RF translator (A1) does not correct the fault, measure voltage levels at P5405 of RF translator A1 (refer to table 3–7). If any voltages measured are incorrect, higher category maintenance is required.

c. If at P5402 the 100-kHz signal measured is not correct, insert signal control card A5 into the transmitter chassis on a 31-pin extender card (para 3–29*b*). Connect oscilloscope 1X probe to J306 pin j on the signal control PC card A5. Set oscilloscope controls as follows:

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				TIME BASE .. 10 μsec/cm VERT ..... 50 mv/cm MAIN SWEEP. NORMAL TRIGGERING . INTERNAL ac A signal level of 30 mv to 100 mv p-p at 100 kHz should be observed. (1) If the signal at J306 pin j is present, replace or repair the coaxial cable between J306 pin j and RF translator A1 P5402. (2) If the signal at J306 pin j is not present, set transmitter POWER ON/OFF switch (S1) to OFF and place ohmmeter test leads to J306 pin b (EXCITER KEY) and ground. A ground indication less than 10 ohms should be indicated. (3) Place ohmmeter test leads between J306 pin c (CARRIER ENABLE) and ground. A ground indication less than 10 ohms should be indicated. (4) Set transmitter POWER ON/OFF switch (S1) to ON. Connect oscilloscope probe to J306 pin e. Set oscilloscope controls as follows: TIME BASE. 10 μsec/cm VERT ..... 100 mv/cm MAIN SWEEP. NORMAL TRIGGERING. INTERNAL ac A 100-kHz signal of 350 ±250 mv p-p should be observed. If this signal is not present, replace synthesizer A2 (para 3–29*d*). If the problem still exists, higher category maintenance is required. *d.* If all the indications of the preceding step are correct, replace signal control card A5 (para 3–29*b*).

				e. If replacing the signal control card A5 does not correct the problem, higher category maintenance is required.
	Transmitter Frequency Checks:			
7	Connect a test cable between the counter SIGNAL INPUT AC jack and 20-db attenuator at transmitter output jack J1 (fig. 3–2). At receiver-transmitter test set select the band edge frequencies (from 2.0000 to 29.9999 MHz listed in table 3–5 on FREQUENCY SELECT thumbwheel switches. Deprrss XMTR DTE pushbutton after each frequency is selected.	The frequency indicated on the counter should be the digits selected on the FREQUENCY SELECT thumbwheel switch ±3 Hz.	Frequency out of tolerance	*a.* If the frequency observed is not correct, connect a test cable from counter high frequency plug-in unit to pump input connector P5403 and RF translator (A1). Perform frequency functional test procedure as follows: (1) Preset the thumbwheel switches on the test set to the frequencies shown in table 3–5 (Digit Checks). The pump frequency 10 MHz through 1-kHz digits should follow the sequence given. If any individual digits are not correct, refer to the note in table 3–6 for corrective action. (2) If step (1) does not correct the pump frequency fault, higher category maintenance is required. (3) Connect counter plug-in test cable to 1st L.O. input at P5404 of the RF translator (A1) assembly. The frequency should correspond to those listed in table 3–5 for each selected 100-Hz frequency change of the thumbwheel switch. (4) If the 100-Hz digits are not correct, refer to corrective action note in table 3–6. *b.* If the above step does not correct the 100-Hz digit fault, replace frequency synthesizer (A2) (para 3–29*d*). If problem still exists after replacement of the frequency synthesizer (A2), higher category maintenance is required. *c.* Connect a test cable from counter frequency input to synthesizer jack J3804 (fig. 4–7②). A

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				100-kHz ±0.1-Hz signal should be observed. If signal amplitude is too low for a stable counter presentation, connect jack J3804 to an ac voltmeter input jack (HP 400D or equivalent). Connect the counter frequency input to the voltmeter output jack. The voltmeter range switch may be changed until the counter indication is observed. If the 100-kHz signal is incorrect, replace frequency synthesizer A2 (para 3–29*d*).
	Tune Power Check:			
8	At the test set, set TUNE PWR switch to on (up position) and KEY switch to on (up position). Set NORMAL LEVELS switch to XMTR PWR. Select any frequency between 2 and 29.9999 MHz on the FREQUENCY SELECT thumbwheel switches. Depress XMTR DTE pushbutton.	The NORMAL LEVELS meter should indicate +3 db.	NORMAL LEVELS meter indicates RF power output too low.	*a.* Connect the RF voltmeter with 50-ohm termination to the 20-db attenuator as shown in figure 3–2. The RF voltmeter level should be 0.2 ±0.05 Vrms. If the level is below that required, connect the 50-ohm RF voltmeter probe to P5402 of the RF translator (A1) using a Sealectro to BNC/TNC adapter. The level should be 30 ±10 mVrms at 100 kHz. *b.* If the signal level at P5402 is correct, replace RF translator (A1) (para 3–29*c*). If the signal level at P5402 is not correct, place signal control card A5 on a 31-pin extender card (para 3–29*b*). Place oscilloscope X1 probe to J306 pin e of A5. Set oscilloscope controls as follows: VERT ..... 100 mv/cm HORIZ ..... 10 μsec/cm MAIN SWEEP. NORMAL TRIGGERING. INTERNAL AC A 100-kHz singal with amplitude of 255 ±105 mv p-p should be observed.

				c. If the 100-kHz signal amplitude is correct, perform signal control card A5 ALC adjustment procedure (para 3–28*h*). If readjustment fails to correct problem, replace signal control card A5 (para 3–29*b*).
				d. If replacement of A5 does not correct the malfunction, measure signal control card A5 voltage inputs as shown in table 3–7. If any input signals are not correct, higher category maintenance is required.
	TGC Function Check:			
9	Set the test set PC switch to ON (up position), KEY switch to ON (up position), and TUNE PWR switch to ON (up position). Verify that the TGC switch (S1) located on the transmit gain control A4 PC card (table 3–12) is in the ON position. Connect a dc voltmeter (negative) to the TGC terminal on test set and adjust TGC potentiometer for a −7 Vdc level. *Note:* The +0.75 Vdc level normally connected to the TGC VOLTAGE test point on transmitter front panel should be removed during this test. Connect the 50-ohm RF voltmeter probe to the 20-db attenuator at transmitter jack J1 (fig. 3–2).	The RF voltmeter should indicate 0.2 ±0.05 Vrms.		
10	Set TUNE PWR switch to off (down position) at the test set.	The RF voltmeter should indicate a level below 100 mVrms, and should not be scanning.	*a.* RF voltmeter is scanning	Vary the TGC potentiometer above and below the −7 Vdc level indicated on the dc voltmeter until scanning stops. If the scanning stops and the dc voltmeter level is not −7 ±0.6V, perform the TGC card alignment procedure (para 3–28*e*). If alignment does not correct the problem, replace TGC card A4 (para 3–29*b*).
			b. RF voltmeter does not scan, but indicates a level above 100 mVrms.	Place transmit gain control card A4 on the 31-pin extender card (para 3–29*b*). Connect positive

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				lead of a dc voltmeter to J307 pin Z. A dc level of +5 ±1V should be observed. If the level is correct and TGC will not scan, perform the following steps: *a.* Place dc voltmeter to J307 pin X. A sweeping signal from +0.2V to +3.7 ±0.5 Vdc should occur. If the level is a steady dc level, replace TGC A4 card (para 3–29*b*). *b.* If the dc signal is sweeping and the RF signal is not scanning, higher category maintenance is required.
			c. RF voltmeter scans up past 400 mVrms and resets to 0, and then continues scanning.	*a.* If scanning does not stop, perform TGC alignment procedure (para 3–28*e*). *b.* If TGC alignment does not correct the malfunction, connect the negative lead of a DCVM to J307 pin *h* and the positive lead to ground. The level should be −7 ±0.6V as set by the TGC potentiometer. Remove the test connection from pin *h* and connect it to J307 pin *d*. The level should be between −1.3 and −2.1V. If this level is not correct, higher category maintenance is required.
			d. RF voltmeter stops scanning at a level other than 400 mVrms.	*a.* If the TGC stops at an incorrect RF output level, adjustment of R5 (table 3–12) on the TGC card may be required. If more than two turns of R5 are required either cw or ccw, perform TGC alignment procedure (para 3–28*e*). *b.* If R5 or TGC alignment fails to correct TGC level, higher category maintenance is required.
			e. TGC will not complete cycle (continues scanning) when the EXCITER GAIN on transmitter front panel is changed.	*a.* If EXCITER GAIN control on front panel is changed and TGC will not stop scanning, the RF gain is too

				low. Set EXCITER GAIN control fully cw. Apply a +0.75 Vdc signal to TGC VOLTAGE test point on transmitter front panel. Adjust R69 (table 3–12) on signal control card A5 for a 0.57 Vrms level as observed on the RF voltmeter. Remove the +0.75 Vdc from the TGC VOLTAGE test point. *b.* Depress the XMTR DTE pushbutton on the test set. The TGC should stop when the −7V TGC sample level is applied. *c.* If steps *a* and *b* above do not correct the fault, higher category maintenance is required.
	Modulation Checks:			
11	All the test set and transmitter switch settings of para 3–24*b* should be as stated except for the following: *Note.* Using the test set +0.75 jack, apply +0.75V to the TGC VOLTAGE test jack on the transmitter front panel. *a.* Set AUDIO INPUT CH A2, CH A1, CH B1, CH B2 on the test set to ON and set KEY switch to up. *b.* Connect a test cable with a 1X probe between the vertical INPUT of a test oscilloscope and J306 pin j of signal control card A5 (fig. FO–51①). Set oscilloscope as follows: TRIGGERING ..... MAIN INT SWEEP MODE ..... NORM MAGNIFIER ..... X1 TIME/DIV ..... 10 μs/cm VOLTS/DIV ..... 0.1 *c.* Set OSC LVL at the test set fully cw. *d.* Set OSC select switch on the test set to each channel position (A1, B1, A2 and B2).	Oscilloscope should display a signal for each channel selection as shown in waveform i (fig. 3–4).	Signal amplitude low or loss of modulation signal at channel selected.	*a.* Connect oscilloscope 1X probe to J306 pin U of signal control card A5. See waveform g for signal control modulation input indication (fig. 3–4). *b.* If signal on J306 pin U is correct, perform signal control

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				card A5 alignment (para 3-28*g* and h). *c.* If the alignment in step *b* above fails to correct problem, replace signal control card A5 (para 3-29*b*). *d.* If replacement of signal control card A5 does not correct fault, connect oscilloscope 1X probe to J306 pin W. See waveform h for ACL input indication (fig. 3-4). *e.* If the signal at pin W of J306 is not correct, replace automatic channel loading card A8 (para 3-29*b*). *f.* If replacement of ACL card A8 does not correct the malfunction, higher category maintenance is required. *g.* Select the input test point corresponding to the faulty channel as listed below, and connect oscilloscope to appropriate channel filter pair PC card A3 or A6 input pin:

	Channel	*Conn*	*Pin*
CH A1/B1 filter pair A3	A1	J302	W
	B1	J302	P
CH A2/B2 filter pair A6	A2	J304	W
	B2	J304	P

Set the oscilloscope as follows:

TRIGGERING ..... MAIN INT
SWEEP MODE ..... NORM
MAGNIFIER X1
TIME/DIV 0.2ms/cm
VOLTS/DIV 0.2V/cm

h. Set OSC select switch on the test set to the faulty channel and look for typical waveform (see fig. 3-4, waveform c).

i. If a good signal is present at the filter pair input pin, check the

output of the channel being measured as listed below:

	Channel	Conn	Pin
CH A1/B1 filter pair A3	A1	J302	j
	B1	J302	A
CH A2/B2 filter pair A6	A2	J304	j
	B2	J304	A

j. If the signal is not present at the output of the channel filter pair being measured, replace the channel pair (A3 or A6) (para 3–29*b*).

k. If the signal is not present at filter pair input pin, remove the test connection from the channel being measured. Select the input test point on the dual-balanced modulator corresponding to the faulty channel as listed below, and connect oscilloscope to appropriate input pin.

	Channel	Conn	Pin
Dual-bal mod A7	A1	J301	T
	B1	J301	V
Dual-bal mod A21	A2	J303	T
	B2	J303	V

See waveform (a) for typical waveform (fig. 3–4). If the signal is not present at pin T or V of A7 or A21, higher category maintenance is required (cable or connector problem).

(1) If the signal is present at pin T or V of A7, remove the test connection from pin T or V and connect it to pin L and then to pin b of A7. Set the oscilloscope as follows:

TRIGGERING ..... MAIN INT
SWEEP MODE ..... NORM
MAGNIFIER X1
TIME/DIV ..... 10 ms/cm
VOLTS/DIV ..... 0.1 V/cm

The oscilloscope should display 100 kHz at each pin measured. If the 100 kHz is present at

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				pin L and pin b, measure the output of A7 at pins R (A1) and X (B1). If a signal is not present at pin R and/or pin X of A7, replace dual-balanced modulator A7 (para 3-29*b*). If a signal is present at pin R and/or pin X of A7, higher category maintenance is required. If the 100-kHz signal is not present at pin L and/or b, higher category maintenance is required. (2) If the signal is present at pin T or V of A21, remove the test connection from pin T or V. Select the input test point on dual-balanced modulator A21 corresponding to the faulty channel listed below, and connect the oscilloscope to the appropriate multiplex carrier generator input signal. *Channel* — *Connector* — *Pin* A2 — J303 — L B2 — J303 — b Set the oscilloscope as follows: TRIGGERING — INT. SWEEP MODE — NORM MAGNIFIER — X1 TIME/DIV — 5 μsec/cm VOLTS/DIV — 0.2 The oscilloscope should display 106.29 kHz at pin L (see waveform (d)), or 93.71 kHz at pin b (see waveform (e), (fig. 3-4). (*a*) If the waveforms are present at pins L and B of A21, measure the output of A21 at pins X (B2) and/or R (A2). If signal is not present at pin X and/or R of A21, replace channel A2, B2 dual-balanced modulator A21 (para 3-29*b*). If a signal is present at pins X and R of A21, a higher

			category maintenance is required. (*b*) If the waveforms are not present at pins L and/or b of dual-balanced modulator A21, measure the output of multiplex carrier generator A9 at pin *d* or F of A9. If a waveform is not persent, replace multiplex carrier generator A9 (para 3–29*b*). (*c*) If the waveform is present at pin *d* or F of A9, higher category maintenance is required.

3-25. Voltage and Frequency Measurements

Voltage and frequency measurements for transmitter assemblies and plug-in PC cards are provided in table 3-7. Only those key input/output signals, control voltage levels, and supply voltages which function as an aid in troubleshooting are listed. These measurements are made with the transmitter on the bench, the top and bottom covers removed, and the transmitter connected to the receiver-transmitter test set (Raytheon part No. T324732A). All measurements are made with the applicable assembly or PC card installed in the transmitter chassis and power on. Instructions are provided in the *Notes* column of table 3-7 wherever special operating conditions are required to obtain measurements listed. All voltage measurements are referenced to transmitter chassis ground unless otherwise specified. When either of two voltage levels may be present at a given pin, both levels are listed in the *Voltage* column and are divided by a slash. Corresponding operating conditions or switch settings are provided in the *Notes* column and are also divided with a slash. As shown in the example below, +19.5V should be present on pin F during AFC OFF condition, and $<+0.3$V should be present during AFC ON condition.

Example:

Pin	Voltage	Notes
F	+19.5 V/$<+0.3$ V	AFC OFF/ AFC/ON

Note: The symbol $<$ means less than.
The symbol $>$ means greater than.

Examples: <-2 V means a voltage less than (or more positive than) -2V (for example -1V).

>-2V means a voltage greater than (or more negative than) -2V (for example -3V).

a. Measurements are made using the following test equipment:

(1) Dc voltages are measured using a differential voltmeter ME-202/U.

(2) Ac voltages are measured using a RMS voltmeter ME-30A/U, or oscilloscope AN/USM-281.

(3) Frequencies are measured using a frequency counter AN/USM-207.

(4) RF voltages are measured using an RF voltmeter AN/URM-145.

CAUTION

To prevent permanent damage to the RF translator (A1) assembly output transistor, insure that a 50-ohm termination (20-db fixed attenuator) is connected to the transmitter output connector J1.

b. With transmitter and test set power off, connect the test setup as shown in figure 3-2.

c. Set the test set controls as listed below.

Control/Indicator	*Setting*
PWR-SET switch	SET (up position)
PWR indicator	illuminated
PWR-XMTR switch	XMTR (up position)
PC ON switch	down position (off)
KEY switch	up position (on)
TUNE PWR switch	down position (off)
AUDIO INPUT CH A1	down position (off)
AUDIO INPUT CH A2	down position (off)
AUDIO INPUT CH B1	down position (off)
AUDIO INPUT CH B2	down position (off)
PC-LVL control	midrange
FREQUENCY SELECT switches.	set to 02.5000 MHz
OSC-LVL control	midrange
OSC select switch	OFF

d. Set the transmitter controls as listed below.

Control/Indicator	*Setting*
EXCITER GAIN control	10
CARRIER ADJUST-LOCAL switch.	REMOTE
CARRIER ADJUST-LOCAL-STEP (-db) switch.	0
TGC ON/OFF switch	OFF (see table 3-12)
ALC ON/OFF switch	ON (see table 3-12)
TGC VOLTAGE jack	Apply +0.75 ±0.05 Vdc.
POWER ON/OFF switch	ON

NOTE

XMTR DTE indicator on the test set illuminates for 10 seconds or less when transmitter POWER ON/OFF switch is set in the ON position.

e. Using a differential voltmeter, measure transmitter power supply voltages, -20, $+20$, and $+6.4$ Vdc on the signal control PC card A5. See table 3-7 signal control PC card A5, for pin numbers and voltage tolerances.

f. Set the testset RCVR XMTR NORMAL LEVELS switch to XMTR A1.

g. Set the test set OSC switch to A1, set XMTR CH A1 switch to the up position, and adjust OSC-LVL control for a -6 dbm reading on the NORMAL LEVELS meter.

h. Adjust the appropriate MODULATION LEVEL –A1, A2, B1, or B2 control on the transmitter front panel fully cw.

i. Repeat steps *f* through *h* for above channels A2, B1 and B2.

NOTE

When performing measurements from table 3–7, figure FO–46 (transmitter interconnection diagram) should be referenced to trace signal flow.

Table 3–7. Voltage and Frequency Measurements

Test point XA	Test point Pin	Signal name	Voltage	Frequency	Notes
		Filter Pair A1/B1 and A2/B2 PC Cards, A3 and A6			
J302, and J304	W	A1 Input/A2 Input	120 ±20 mv p-p	100 kHz modulated	See waveform (c) fig. 3–4.
	P	B1 Input/B2 Input	120 ±20 mv p-p	100 kHz modulated	
	j	A1 Output/A2 Output	25 ±5 mv p-p	100 kHz nominal	See waveform (f) fig. 3–4.
	A	B1 Output/B2 Output	25 ±5 mv p-p	100 kHz nominal	
		Transmit Gain Control PC Card A4			
07	*a*	−5V rgltd	−5 ±1V		
	B	+6.4V	+6.4 ±0.05V		
	A	+20V	+20 ±0.1V		
	C	−28V unrgltd	−28 +3, −10V		
	h	TGC sample in	0V to −7 ±0.6V		
	d	TGC reference	−1.3V to −2.1V		
	P	Digital tune enable	Gnd/+9 ±1V		XMTR DTE pushbutton depressed/not tuning.
	M	Synthesizer tune enable	Gnd/+10V		
	Z	Memory reset	<+0.4/>+3V pulse		See waveform (l) fig. 3–4.
	V	Reset output	0V/+4 ±0.5V pulse		
	X	D/A output	+0.2V/+3.7 ±0.5V		See waveform (k) fig. 3–4.
	k	−20V	−20 ±0.1V		
		Signal Control PC Card A5			
J306	A	+20V	+20 ±0.1V		
	H	−20V	−20 ±0.1V		
	C	−28V	−28 +3, −10V		
	B	+6.4V	+6.4V ±0.05V		
	b	Exciter key	0V/+6.3V		KEY switch up/ KEY switch down.
	Z	TGC reference	−3.3 ±0.05V		
	K	A1 output	25 ±5 mv p-p		See waveform (f) fig. 3–4.
	N	B1 output	25 ±5 mv p-p		
	P	A2 output	25 ±5 mv p-p		See waveform (f) fig. 3–4.
	T	B2 output	25 ±5 mv p-p		
	J	Tune enable	+19.5 ±0.5V/<+0.3V		TUNE PWR switch down/ TUNE PWR switch up.
	F	ALC sample	0V to −10V		
	e	100-kHz carrier	60 to 300 mv rms	100 kHz ±0.1 Hz	Externally applied voltage.
	U	ACL	15 ±4 mv p-p		See waveform (g) fig. 3–4.
	Y	Tune leveler	+3 ±0.6V		TUNE PWR switch up.
	W	Multiplex input	6 ±2 mv p-p		See waveform (h) fig. 3–4.
	j	Output	50 ± mv p-p	100 kHz nominal	See waveform (i) fig. 3–4.
					Adjust MODULATION LEVEL −A1, A2, B1 or B2

	a.	D/A output	<1V to >3.4V p-p sawtooth waveform		control for 0.45 Vrms at 20-db attenuator output at J1. Set TGC switch to on, remove +0.75 Vdc from TGC VOLTAGE jack and observe scan. See waveform (k) fig. 3–4.
		Dual-Balanced Modulator A1/B1 and A2/B2 PC Cards, A7 and A21			
J301, and J303	A	+20V	+20 ±0.1V		
	L (J301)	100-kHz carrier	60 to 300 mVrms	100 kHz ±0.1 Hz	See waveforms (b), (*d*), and (e), fig. 3–4.
	L (J303)	106.29-kHz carrier	70 ±10 mVrms	106.29 kHz ±5 Hz	
	H to K	Audio Input (ch A)	1.2 ±0.2V p-p		
	J	Audio in (ch A) xfmr C.T.	0.6 ±0.1V p-p		
	T	Adjust audio input (ch A)	0.3 ±0.04V p-p		See waveform (a) fig. 3–4.
	E	Audio out (ch A) to gain control	0.3 ±0.04V p-p		
	R	Balanced modulator out (ch A)	125 ±15 mV p-p		See waveform (c) fig. 3–4.
	c to *e*	Audio input (ch B)	1.2 ±0.2V p-p		
	d	Audio in (ch B) xfmr C.T.	0.6 ±0.1V p-p		
	V	Adjust audio input (ch B)	0.3 ±0.04V p-p		See waveform (a) fig. 3–4.
	j	Audio out (ch B) to gain control	0.3 ±0.04V p-p		
	X	Balanced modulator out (ch B)	125 ±15 mv p-p		See waveform (c) fig. 3–4.
	b (J301)	100-kHz carrier	60 to 300 mv p-p	100 kHz ±0.1 Hz	See waveforms (b),(d), and (e) fig. 3–4.
	b (J303)	93.71-kHz carrier	70 ±10 mv p-p	93.71 kHz ±5 Hz	
		Automatic Channel Loading (ACL) PC Card A8			
J314	A	+20V	+20 ±0.1V		
	F	−20V	−20 ±0.1V		
	K	Rf translator detector	+4 ±1V		Adjust MODULATION LEVEL –A1, A2, B1, or B2 control for 0.45 Vrms at 20-db attenuator output at J1.
	J	Tune enable	+19.5 ±0.5V/<0.3V		TUNE PWR down/TUNE PWR up.
	P	Combined signal	6 ±2 mV p-p		See waveform (h), fig. 3–4.
	N	D/A output	<1V to >3.4V p-p sawtooth waveform		Adjust MODULATION LEVEL–A1, A2, B1 or B2 control for 0.45 Vrms at 20-db attenuator output at J1. Set TGC switch to on, remove +0.75 Vdc from TGC VOLTAGE jack and observe scan. See waveform (k) fig. 3–4.
	R	Channel B2 enable	<+0.3V/+13.6 ±1V		CH B2 switch up/ CH B2 switch down

Test point XA	Test point Pin	Signal name	Voltage	Frequency	Notes
	S	Channel B1 enable	<+0.3V/+13.6 ±1V		CH B1 switch up/ CH B1 switch down
	T	Channel A2 enable	<+0.3V/+13.6 ±1V		CH A2 switch up/ CH A2 switch down
	U	Channel A1 enable	<+0.3V/+13.6 ±1V		CH A1 switch up/ CH A1 switch down
	C	Rf detector output	+0.4 ±0.2V		*Note.* Only one channel enable switch should be up at a time.
	L	Signal control ACL	15 ±4 mv p-p		Set TUNE PWR switch up. To observe signal control ACL signal at pin L, adjust MODULATION LEVEL–A1, A2, B1, or B2 control for 0.45 Vrms at 20-db attenuator output at J1. See waveform (g) fig. 3–4.
	H	Signal control tune leveler	+3 ±0.6V		
	B	RF translator (AGC control)	+2.9 ±0.3V		
	V	Exciter gain control front panel adjust	+15 ±1V		
	M	Exciter gain control front panel adjust	+7.5 ±0.6V		
Multiplex Carrier Generator (MCG) PC Card A9					
J305	A	+20V	+20 ±0.1V		
	F	93.71-kHz oscillator out	70 ±10 mVrms	93.7 kHz ±5 Hz	See waveform (e) fig. 3–4.
	d	106.29-kHz oscillator out	70 ±10 mVrms	106.29 kHz ±5 Hz	See waveform (d) fig. 3–4
Frequency Select Memory PC Cards A13, A14, and A15					
J308, J309, and J310	S	Set input No. 1	<+0.8V pulse/>+25V level		A test set no code input pulse will be +3.2V nominal instead of a +28 −Vdc level. Select various codes into FREQ SEL switches and depress XMTR TUNE pushbutton each time to observe code line voltage levels. For input pulse waveform see waveforms (n) and (o) fig. 3–4. Refer to table 2–1 for frequency select input codes. Refer to the receiver interconnection diagram (fig. FO–46) for pin number conversions. *Note.* "0" = > +25V level. "1" = < +0.8V pulse.
	P	Set input No. 2	<+0.8V pulse/>+25V level		
	M	Set input No. 3	<+0.8V pulse/>+25V level		
	K	Set input No. 4	<+0.8V pulse/>+25V level		
	H	Set input No. 5	<+0.8V pulse/>+25V level		
	W	Set input No. 6	<+0.8V pulse/>+25V level		
	Y	Set input No. 7	<+0.8V pulse/>+25V level		
	a	Set input No. 8	<+0.8V pulse/>+25V level		
	c	Set input No. 9	<+0.8V pulse/>+25V level		
	e	Set input No. 10	<+0.8V pulse/>+25V level		
	T	Output No. 1	>+3.5V/<+0.2V		
	R	Output No. 2	>+3.5V/<+0.2V		
	N	Output No. 3	>+3.5V/<+0.2V		
	L	Output No. 4	>+3.5V/<+0.2V		
	J	Output No. 5	>+3.5V/<+0.2V		
	V	Output No. 6	>+3.5V/<+0.2V		
	X	Output No. 7	>+3.5V/<+0.2V		
	Z	Output No. 8	>+3.5V/<+0.2V		
	b	Output No. 9	>+3.5V/<+0.2V		
	d	Output No. 10	>+3.5V/<+0.2V		

	B	+6.4V input	+6.4 ±0.05V		
	h	Reset	<+0.4/>+3.0V pulse		See waveform (1) fig. 3–4.
		Band Control PC Card A16			
J311	34, 38, 39, 40, 41	1's MHz in	<+0.3V/>+3.5V		See table below for voltages measured at pins 1 and 13:
	14, 17, 18	10's MHz in	<+0.3V/>+3.5V		
	7, 8, 9, 10, 11 12	100's MHz in	<+0.3V/>+3.5V		
	1	1–6-MHz VCO band B	See note		
	13	1–6-MHz VCO band C	See note		
	31	2–6.9-MHz hf VCO band 1	<+0.3V/>+5V		
	32	7–11.9-MHz hf VCO band 2	<+0.3V/>+5V		
	27	12–16.9-MHz hf VCO band 3	<+0.3V/>+5V		Refer to tables 3–8 and 3–9 for input codes.
	24	17–21.9-MHz hf VCO band 4	<+0.3V/>+5V		
	22	22–26.9-MHz hf VCO band 5	<+0.3V/>+5V		
	20	27–29.9-MHz hf VCO band 6	<+0.3V/>+5V		
	37	2–2.9-MHz preset band	<+0.3V/>+5V		
	35	2–4.9-MHz preset band	<+0.3V/>+5V		
	33	5–6.9-MHz preset band	<+0.3V/>+5V		
	29	7–9.9-MHz preset band	<+0.3V/>+5V		
	28	10–14.9-MHz preset band	<+0.3V/>+5V		
	25	15–21.9-MHz preset band	<+0.3V/>+5V		
	21	22–29-MHz preset band	<+0.3V/>+5V		
	5	1–6-MHz VCO band I + 4	<+0.3V/>+4V		
	19	1–6-MHz VCO band II + 2	<+0.3V/>+4V		
	6	1–6-MHz VCO band III + 1	<+0.3V/>+4V		
	2	+6.4v	+6.4 ±0.05V		

1–6 MHz VCO bands selected	*Pin 1*	*Pin 13*
B.C	<+0.3V	+12 ± 1.5V
B.C	+12 ± 1.5V	<+0.3V
B.C	>+19.V	>+19.V

		Code Conversion Matrix No. 1 PC Card A17			
J312	F, H, J, K, L	100's of kHz input	>+3.6V/<+0.3V		Refer to table 3–10 for input/output codes.
	N, P, R, S	100's of kHz output to VDSP	>+3.6V/<+0.3V		
	C, D, *f*, *j*, *z*	100's of kHz output to band control	>+3.6V/<+0.3V		
	e, *d*, *c*, *b*, *a*	10's of kHz input	>+3.6V/<+0.3V		
	X, W, V, U	10's of kHz output to VDSP	>+3.6V/<+0.3V		
	B	+6.4V input	+6.4 ±0.05V		

Test point XA	Test point Pin	Signal name	Voltage	Frequency	Notes
		Code Conversion Matrix No. 2 PC Card A18			
J313	*e, d, c, b, a*	Units of kHz input	>+3.6V/<+0.3V		Refer to table 3–10 for input/output codes.
	U, V, W, X	Units of kHz output to VDSP	>+3.6V/<+0.3V		
	F, H, J, K, L	100's of Hz input	>+3.6V/<+0.3V		
	S, R, P, N, M	100's of Hz output to 2nd L.O. var div	>+3.6V/<+0.3V		
	B	+6.4V input	+6.4 ±0.05V		
		RF Translator Assembly A1			
J5401		Transmitter output	4.5 Vrms	2 to 30 MHz	See waveforms (j) and (m) fig. 3–4.
J5402		100-kHz input	50 ±10 mv p-p	100 kHz nominal	See waveform (i) fig. 3–4.
J5403		61–89-MHz input	160 to 340 mVrms	61–89 MHz	
J5404		90.9-MHz input	25 to 45 mVrms	90.8990 to 90.8999 MHz	
P5405	1	Gnd			
	2	−28 Vdc unrgltd	−28 +3, −10V		
	3	+20 Vdc	+20 ±0.1V		
	4	Gnd			
	5	Det output	N/A		
	6	AGC control	+2.7 to +7.6 Vdc		
		Frequency Synthesizer Assembly A2			
J3804		100-kHz reference	60 to 300 mVrms	100 kHz nominal	
J3805		61–89 MHz output	160 to 340 mVrms	61–89 MHz	
J3807		90.889-MHz output	25 to 45 mVrms	90.8990 to 90.8999 MHz	
P3801	1	2–6.9-MHz input	<+0.4V/+6±0.4V		Refer to table 2–5 for codes applicable to pins 1 through 11.
	2	7–11.9-MHz input	<+0.4V/+6±0.4V		
	3	12–16.9-MHz input	<+0.4V/+6±0.4V		
	4	17–21.9-MHz input	<+0.4V/+6±0.4V		
	5	22–26.9-MHz input	<+0.4V/+6±0.4V		
	6	27–29.9-MHz input	<+0.4V/+6±0.4V		
	8	1–6-MHz VCO + 4 input	<+0.3V/>+3V		
	10	1–6-MHz VCO + 2 input	<+0.3V/>+3V		
	11	1–6-MHz VCO + 1 input	<+0.3V/>+3V		
	12	Units of MHz	<+0.3V/>+3V		Refer to tables 3–8 through 3–10 for codes applicable to pins 12 through 34. Also refer to the transmitter interconnection diagram (fig. FO–46) for pin number conversions.
	13	Units of MHz	<+0.3V/>+3V		
	14	Units of MHz	<+0.3V/>+3V		
	16	Hundreds of kHz	<+0.3V/>+3V		
	17	Hundreds of kHz	<+0.3V/>+3V		
	18	Hundreds of kHz	<+0.3V/>+3V		
	19	Hundreds of kHz	<+0.3V/>+3V		
	21	Tens of kHz	<+0.3V/>+3V		
	22	Tens of kHz	<+0.3V/>+3V		
	23	Tens of kHz	<+0.3V/>+3V		

24	Tens of kHz	<+0.3V/>+3V		
25	Units of kHz	<+0.3V/>+3V		
26	Units of kHz	<+0.3V/>+3V		
27	Units of kHz	<+0.3V/>+3V		
28	Units of kHz	<+0.3V/>+3V		
30	Hundreds of Hz	<+0.3V/>+3V		
31	Hundreds of Hz	<+0.3V/>+3V		
32	Hundreds of Hz	<+0.3V/>+3V		
33	Hundreds of Hz	<+0.3V/>+3V		
34	Hundreds of Hz	<+0.3V/>+3V		
35	Digital tune in progress	+28V nominal		
40	+6.4V	+6.4 ±0.05V		
41	−28V unrgltd	−28 +3, −10V		
42	+20V	+20 ±0.1V		
43	Gnd			
44	−20V	−20 ±0.2V		
45	Gnd			
49	+27 Vdc (system)	+27V nominal		
50	1–6-MHz VCO band B	<+1.0V		
47	1–6-MHz VCO band C	<+1.0V		
46	DTE	0V/2.5±1V		XMTR DTE pushbutton depressed/not tuning.
		−28V Power Supply A19		
1, 2 5	120 Vac input −28 Vdc output	120 Vac ±10% −28 +3, −10 Vdc nominal (115 Vac, 60 Hz input)	47–420 Hz	
		+20V Power Supply A11		
1, 2 6, 7	120 Vac input +20 Vdc output	120 Vac ±10% +20 ±0.1 Vdc	47–420 Hz	
		+6.4V Power Supply A10		
1, 2 6, 7	120 Vac input +6.4 Vdc output	120 Vac ±10% +6.4 ±0.05 Vdc	47–420 Hz	

Table 3-8. Band Control Card A16 Signal Inputs Tens-of-MHz Signal Inputs

Selected frequency	14	18	17
2.0 – 9.9	–	x	x
10.0 – 19.9	x	x	–
20.0 – 29.9	x	–	x

Units-of-MHz signal inputs

Selected frequency	41	40	39	38	34
0.0 – 0.9	–	x	–	–	x
1.0 – 1.9	x	x	–	–	–
2.0 – 2.9	x	–	x	–	–
3.0 – 3.9	–	x	x	–	–
4.0 – 4.9	–	x	–	x	–

Units-of-MHz signal inputs

5.0 – 5.9	–	–	x	x	–
6.0 – 6.9	–	–	x	–	x
7.0 – 7.9	–	–	–	x	x
8.0 – 8.9	x	–	–	x	–
9.0 – 9.9	x	–	–	–	x

NOTES

1. Pin numbers in headings are those of connector J311.
2. x denotes +5 Vdc present at pin.
3. –denotes ground present at pin.

Table 3-9. Band Control Card A16, Signal Outputs

Selected frequency	Units-of-MHz output			Hf VCO preselect band	Harmonic generator injection frequency	Mixer injection and VCO band control outputs data					
Pins	16	15	3			31	32	27	24	22	20
2.0 – 2.9	x	–	–	1	90	x	–	–	–	–	–
3.0 – 3.9	–	x	x	1	90	x	–	–	–	–	–
4.0 – 4.9	–	x	–	1	90	x	–	–	–	–	–
5.0 – 5.9	–	–	x	1	90	x	–	–	–	–	–
6.0 – 6.9	–	–	–	1	90	x	–	–	–	–	–
7.0 – 7.9	x	–	–	2	85	–	x	–	–	–	–
8.0 – 8.9	–	x	x	2	85	–	x	–	–	–	–
9.0 – 9.9	–	x	–	2	85	–	x	–	–	–	–
10.0 – 10.9	–	–	x	2	85	–	x	–	–	–	–
11.0 – 11.9	–	–	–	2	85	–	x	–	–	–	–
12.0 – 12.9	x	–	–	3	80	–	–	x	–	–	–
13.0 – 13.9	–	x	x	3	80	–	–	x	–	–	–
14.0 – 14.9	–	x	–	3	80	–	–	x	–	–	–
15.0 – 15.9	–	–	x	3	80	–	–	x	–	–	–
16.0 – 16.9	–	–	–	3	80	–	–	x	–	–	–
17.0 – 17.9	x	–	–	4	75	–	–	–	x	–	–
18.0 – 18.9	–	x	x	4	75	–	–	–	x	–	–
19.0 – 19.9	–	x	–	4	75	–	–	–	x	–	–
20.0 – 20.9	–	–	x	4	75	–	–	–	x	–	–
21.0 – 21.9	–	–	–	4	75	–	–	–	x	–	–
22.0 – 22.9	x	–	–	5	70	–	–	–	–	x	–
23.0 – 23.9	–	x	x	5	70	–	–	–	–	x	–
24.0 – 24.9	–	x	–	5	70	–	–	–	–	x	–
25.0 – 25.9	–	–	x	5	70	–	–	–	–	x	–
26.0 – 26.9	–	–	–	5	70	–	–	–	–	x	–
27.0 – 27.9	x	–	–	6	65	–	–	–	–	–	x
28.0 – 28.9	–	x	x	6	65	–	–	–	–	–	x
29.0 – 29.9	–	x	–	6	65	–	–	–	–	–	x

NOTES

1. Pin numbers in heading are those of connector J311.
2. x denotes +5 Vdc present at pin.
3. –denotes ground present at pin.

Table 3-10. Code Conversion Matrix Cards A17 and A18 Signal Inputs and Outputs

Digits	Inputs F e	H d	J c	K b	L a	Outputs to VDSP: Units of kHz matrix No. 2 / 10's of kHz matrix No. 1 / 100's of kHz matrix No. 1	X X N	W W P	V V R	U U S	Output to band control: Matrix no. 1	C	D	f	A	j	Z	Output to 2nd L.O.: Matrix no. 2	S	R	P	M	N
0	–	x	–	–	x	0	x	–	–	x	0	–	–	–	x	x	–	0	–	–	–	–	–
1	x	x	–	–	–	1	x	–	–	–	1	–	–	–	x	x	–	1	–	–	–	–	x
2	x	–	x	–	–	2	–	x	x	x	2	–	–	x	–	x	–	2	–	–	–	x	x
3	–	x	x	–	–	3	–	x	x	–	3	–	–	x	–	x	–	3	–	–	x	x	x
4	–	x	–	x	–	4	–	x	–	x	4	–	–	x	–	–	x	4	–	x	x	x	x
5	–	–	x	x	–	5	–	x	–	–	5	–	x	–	–	–	x	5	x	x	x	x	x
6	–	–	x	–	x	6	–	–	x	x	6	–	x	–	–	–	x	6	x	x	x	x	–
7	–	–	–	x	x	7	–	–	x	–	7	–	x	–	–	–	x	7	x	x	x	–	–
8	x	–	–	x	–	8	–	–	–	x	8	x	x	–	–	–	x	8	x	x	–	–	–
9	x	–	–	–	x	9	–	–	–	–	9	x	x	–	x	–	x	9	x	–	–	–	–

NOTES

1. Pin letters in headings are the same for connector J312 or J313.
2. x denotes +5 vdc present at pin.
3. –denotes ground present at pin.
4. Code conversion matrix card No. 1 contains circuits for 100's-and 10's-of-kHz (J312). Card No. 2 contains circuits for units-of-kHz and 100's-of-Hz (J313).

3-26. Waveforms
(figs. 3-3 and 3-4)

Typical waveforms of signals at key test points within the transmitter are provided to aid in fault isolation. These waveforms are measured with the transmitter on the bench, the top and bottom covers removed, and the transmitter connected to the receiver-transmitter test set (Raytheon part No. T324732A). Figure 3-3 provides a simplified block diagram of the transmitter showing test point locations for each waveform in figure 3-4. Figure 3-4 provides actual oscilloscope waveform pictures which show typical amplitude, frequency, and noise level characteristics. Waveforms are viewed using a Tektronix 545A oscilloscope with a type 53/54B plug-in. Applicable oscilloscope settings and test point information is given for each waveform.

NOTE

These waveforms are intended for use as visual troubleshooting aids only, and are not to be used as performance standards. For specific amplitude and frequency tolerances, refer to voltage and frequency measurements (table 3-7).

CAUTION

To prevent permanent damage to the RF translator (A1) assembly output transistor, insure that a 50-ohm termination (20-db fixed attenuator) is connected to the transmitter output connector J1.

a. With transmitter and test set power off, connect the test setup as shown in figure 3-2.

b. Set the test set controls as listed below.

Control/indicator	*Setting*
PWR-SET switch	SET (up position)
PWR indicator	illuminated
PWR-XMTR switch	XMTR (up position)
PC ON switch	down position (off)
KEY switch	up position (on)
TUNE PWR switch	down position (off)
AUDIO INPUT CH A1	down position (off)
AUDIO INPUT CH A2	down position (off)
AUDIO INPUT CH B1	down position (off)
AUDIO INPUT CH B2	down position (off)
PC-LVL control	midrange
FREQUENCY SELECT switches.	set to 02.5000 MHz
OSC-LVL control	midrange
OSC select switch	OFF

c. Set the transmitter controls as listed below.

Control/indicator	*Setting*
EXCITER GAIN control	10
CARRIER ADJUST-LOCAL switch.	REMOTE
CARRIER ADJUST-LOCAL-STEP (–db) switch.	0
TGC ON/OFF switch	OFF (see table 3-12)
ALC ON/OFF switch	ON (see table 3-12)
TGC VOLTAGE jack	Apply +0.75 ±0.05 Vdc
POWER ON/OFF switch	ON

NOTE

XMTR DTE indicator on test set illuminates for 10 seconds or less when transmitter POWER ON/OFF switch is set to the ON position.

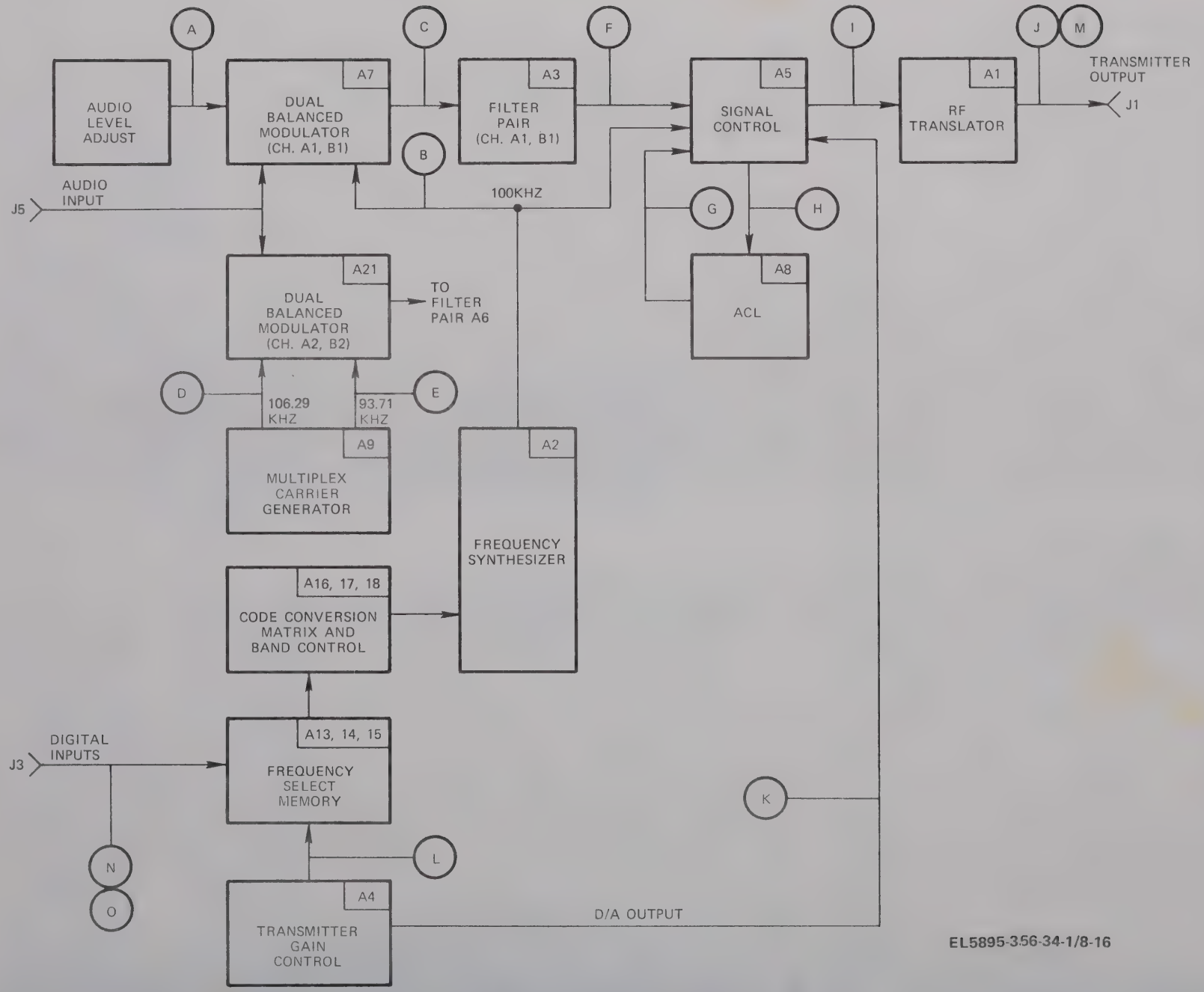
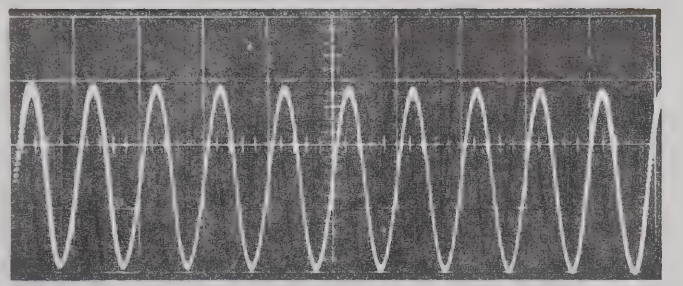


Figure 3–3. Transmitter troubleshooting, waveforms guide.

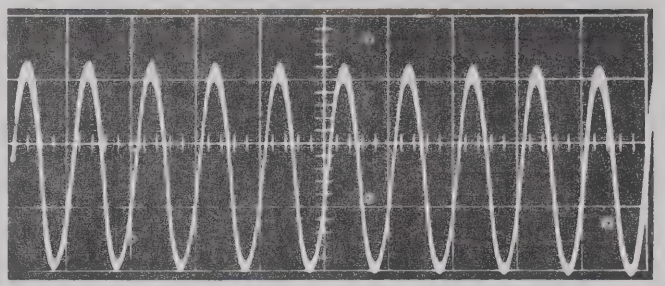
(A)



TEST POINT: J301-T, V; J303-T, V
OSCILLOSCOPE SETTINGS: 0.1V/CM, 1 MSEC/CM,
INT AC TRIGGER

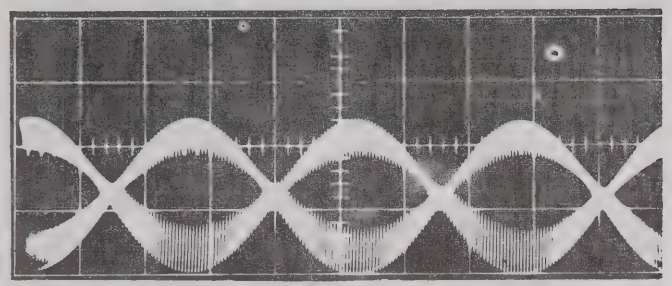
APPLY AUDIO OSCILLATOR INPUT SIGNAL OF 1 KHZ,
-6 DBM TO AUDIO INPUT PINS H AND K OR C AND E;
AND ADJUST MODULATION LEVEL CONTROL FULLY CW.

(B)



TEST POINT: J301-B, J306-C
OSCILLOSCOPE SETTINGS: 0.1V/CM, 10 μ SEC/CM,
INT AC TRIGGER

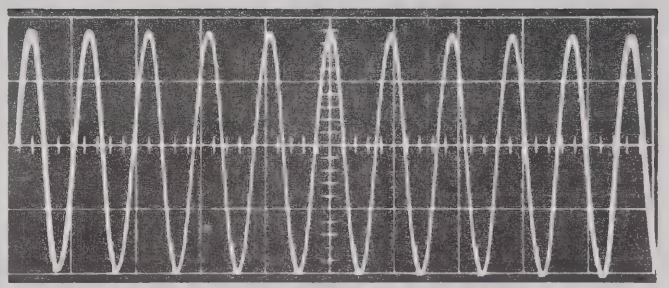
(C)



TEST POINT: J301-R, X; J303-R, X
OSCILLOSCOPE SETTINGS: 0.05V/CM, 0.2 MSEC/CM,
INT AC TRIGGER

SET APPROPRIATE XMTR CHAN A1, A2, B1, B2 SWITCH TO
UP POSITION ONE AT A TIME TO OBSERVE EACH CHANNEL.

(D)

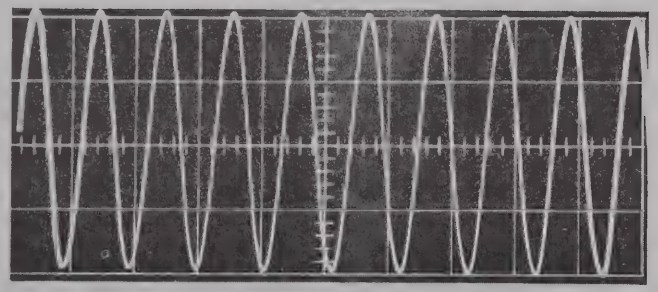


TEST POINT: J303-L
OSCILLOSCOPE SETTINGS: 0.05V/CM, 10 μ SEC/CM,
INT AC TRIGGER

EL5895—356—34—1/8—17 ①

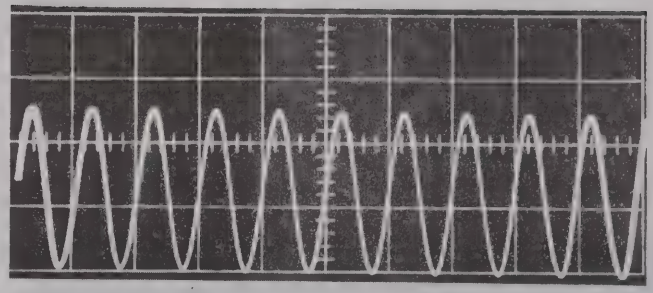
Figure 3-4①. Transmitter troubleshooting, waveforms (sheet 1 of 4).

(E)



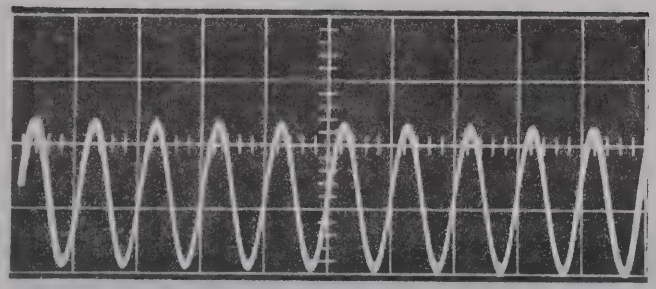
TEST POINT: J303-B
OSCILLOSCOPE SETTINGS: 0.05V/CM, 10 μ SEC/CM, INT AC TRIGGER

(F)



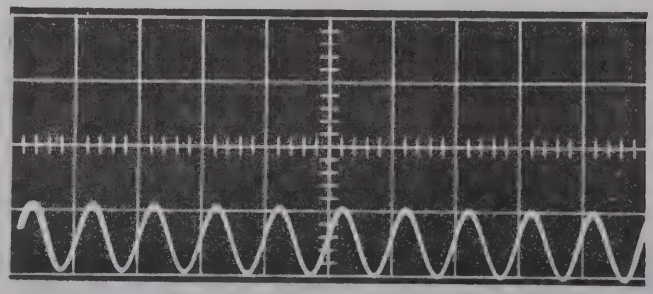
TEST POINT: J302-J, A; J304-J, A
OSCILLOSCOPE SETTINGS: 0.01V/CM, 10 μ SEC/CM, INT AC TRIGGER

(G)



TEST POINT: J306-U
OSCILLOSCOPE SETTINGS: 0.005V/CM, 10 μ SEC/CM, INT AC TRIGGER

(H)

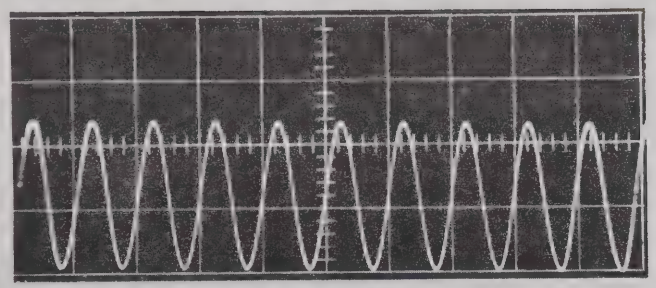


TEST POINT: J306-W
OSCILLOSCOPE SETTINGS: 0.005V/CM, 10 μ SEC/CM, INT AC TRIGGER

EL5895—356—34—1/8—17 ②

Figure 3-4②. Transmitter troubleshooting, waveforms (sheet 2 of 4).

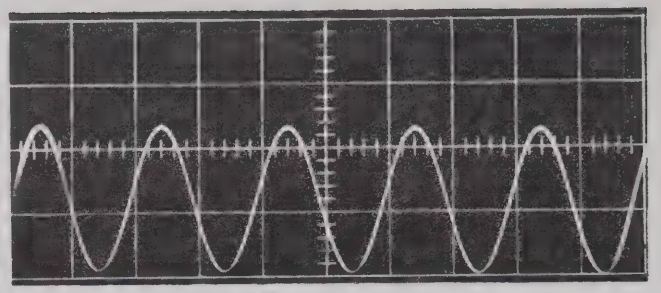
(I)



TEST POINT: J306-J
OSCILLOSCOPE SETTINGS: 0.02V/CM, 10 μ SEC/CM, INT AC TRIGGER

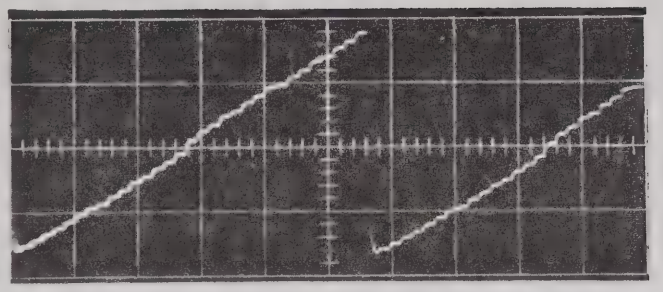
ADJUST MODULATION LEVEL - A1, A2, B1, OR B2 CONTROL FOR 0.45V VRMS AT ATTENUATOR OUTPUT AT J1.

(J)



TEST POINT: J1 (UNMODULATED OUTPUT)
OSCILLOSCOPE SETTINGS: 5V/CM, 0.2 μ SEC/CM, INT AC TRIGGER

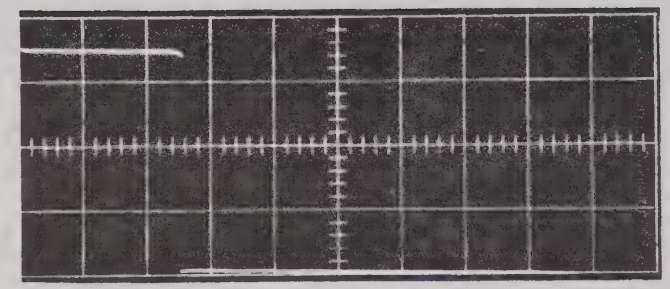
(K)



TEST POINT: J307-X
OSCILLOSCOPE SETTINGS: 1V/CM, 1 SEC/CM, DC INT POS TRIGGER

SET TGC SWITCH TO ON, REMOVE 0.75VDC FROM TGC VOLTAGE JACK.

(L)



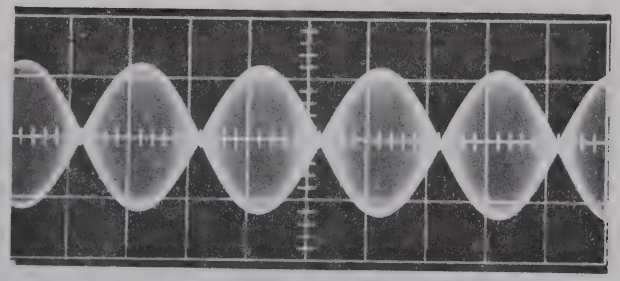
TEST POINT: J307-V
OSCILLOSCOPE SETTINGS: 1V/CM, 20 MSEC/CM, DC INT POS TRIGGER

DEPRESS XMTR DTE PUSHBUTTON TO OBSERVE WAVEFORM.

EL5895—356—34—1/8—17 ③

Figure 3-4③. Transmitter troubleshooting, waveforms (sheet 3 of 4).

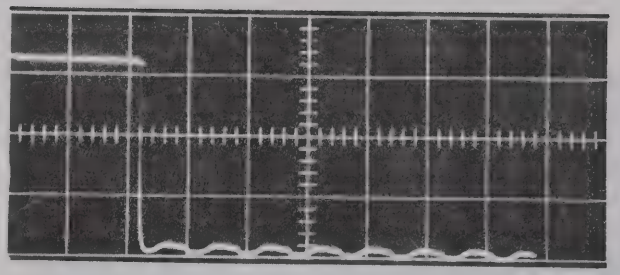
(M)



TEST POINT: J1 (MODULATED OUTPUT)
OSCILLOSCOPE SETTINGS: 5V/CM, 0.5 MSEC/CM, INT AC TRIGGER

APPLY 0.75VDC TO TGC VOLTAGE JACK. ADJUST A1 MODULATION LEVEL CONTROL FOR 2.25VRMS AT J1. SET CARRIER ADJUST LOCAL FUNCTION SWITCH TO AM.

(N)



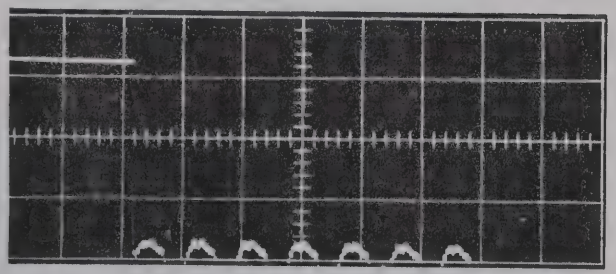
TEST POINT: REFER TO TABLE 3-7
OSCILLOSCOPE SETTINGS: 1V/CM, 20 MSEC/CM, DC INT POS TRIGGER

DIGITAL INPUT CODE LINE NOT SELECTED.

NOTE:
A +28VDC LEVEL IS PRESENT WHEN TRANSMITTER IS RACK MOUNTED.

DEPRESS XMTR DTE PUSHBUTTON TO OBSERVE WAVEFORM.

(O)



TEST POINT: REFER TO TABLE 3-7
OSCILLOSCOPE SETTINGS: 1V/CM, 20 MSEC/CM DC INT POS TRIGGER

DIGITAL INPUT CODE LINE SELECTED.

NOTE:
A +28VDC PULSE IS PRESENT WHEN TRANSMITTER IS RACK MOUNTED.

DEPRESS XMTR DTE PUSHBUTTON TO OBSERVE WAVEFORM.

EL5895-356-34-1/8-17 ④

Figure 3-4④. Transmitter troubleshooting, waveforms (sheet 4 of 4).

d. Using a differential voltmeter, measure transmitter power supply voltages, −20, +20, and +6.4 Vdc on the signal control PC card A5. See table 3–7, signal control PC card A5, for pin numbers and voltage tolerances.

e. Set the test set RCVR XMTR NORMAL LEVELS switch to XMTR A1.

f. Set the test set OSC switch to A1, set XMTR CH A1 switch to up position, and adjust OSC–LVL control for a −6 dbm reading on the NORMAL LEVELS meter.

g. Adjust the appropriate MODULATION LEVEL –A1, A2, B1, or B2 control on the transmitter front panel fully cw.

h. Repeat steps *e* through *g* above for channels A2, B1, and B2.

Section III. MAINTENANCE OF TRANSMITTER

3–27. General

This section contains adjustment, alignment, and removal replacement procedures for the transmitter. In normal operation (when rack installed) the transmitter does not require adjustments or alignments. It is completely aligned at the depot prior to shipment. The adjustments and alignments in this section are provided to return the transmitter to normal operation after replacement of a plug-in card, module or subassembly. The removal and replacement procedures provide removal of the transmitter from its rack installation, and removal of plug-in cards, modules or subassemblies.

3–28. Adjustment and Alignment Procedures

The following adjustment and alignment procedures are performed in conjunction with the troubleshooting procedures. If a malfunction occurs and a plug-in card, module, or subassembly is replaced, adjustment and/or alignment of the unit replaced should be performed to insure proper transmitter operation. Any adjustments not covered in the following procedures, except for front panel controls, are considered to be higher category adjustments. Table 3–11 lists the adjustments and/or alignments covered in this section and when these adjustments and/or alignments are required after replacement of an assembly has been performed. The test setup (fig. 3–2) and switch settings (para 3–24*b*) used in troubleshooting remain the same when performing the adjustment and alignment procedures. Figure 3–5 shows locations of +6.4 Vdc, +20 Vdc, and frequency synthesizer 5-MHz clock adjustments. Table 3–12 references locations of printed circuit card adjustments.

NOTE

If a screwdriver adjustment is sealed with cementing compound, apply Glyptal thinner GC–67 before making adjustment.

Table 3–11. Adjustment and Alignment Procedures

Adjustment and/or alignment	*Performed after replacement of—*
+6.4 Vdc Power supply	+6.4 Vdc power supply A10
+20 Vdc Power supply	+20 Vdc Power supply A11
Signal control card −20 Vdc adjustment.	Signal control card A5
Frequency synthesizer 5-MHz clock.	Frequency synthesizer A2
Transmit gain control	Transmit gain control card A4
Automatic channel loading	Automatic channel loading card A8
Signal control am level	Signal control card A5
Signal control ALC and TGC.	Signal control card A5 RF Translator A1
Automatic load control (ALC).	Transmit gain control A4

a. +6.4 Vdc Power Supply A10 Adjustment. This adjustment is performed with a differential voltmeter and 31-pin extender board A20.

(1) Insure the transmitter POWER ON/OFF switch is OFF.

(2) Install signal control card A5 (fig. FO–51①) into the transmitter chassis assembly using 31-pin extender card A20.

(3) Set the differential voltmeter to measure +10 Vdc.

(4) Connect a test cable between G (ground) on the digital voltmeter and the transmitter chassis.

(5) Connect a test cable between the positive jack of the digital voltmeter and pin B of signal control card A5.

(6) Set the transmitter POWER ON/OFF switch to ON.

(7) Adjust +6.4 Vdc power supply adjustment (fig. 3–5) for a +6.4 ±0.05 Vdc indication on the differential voltmeter.

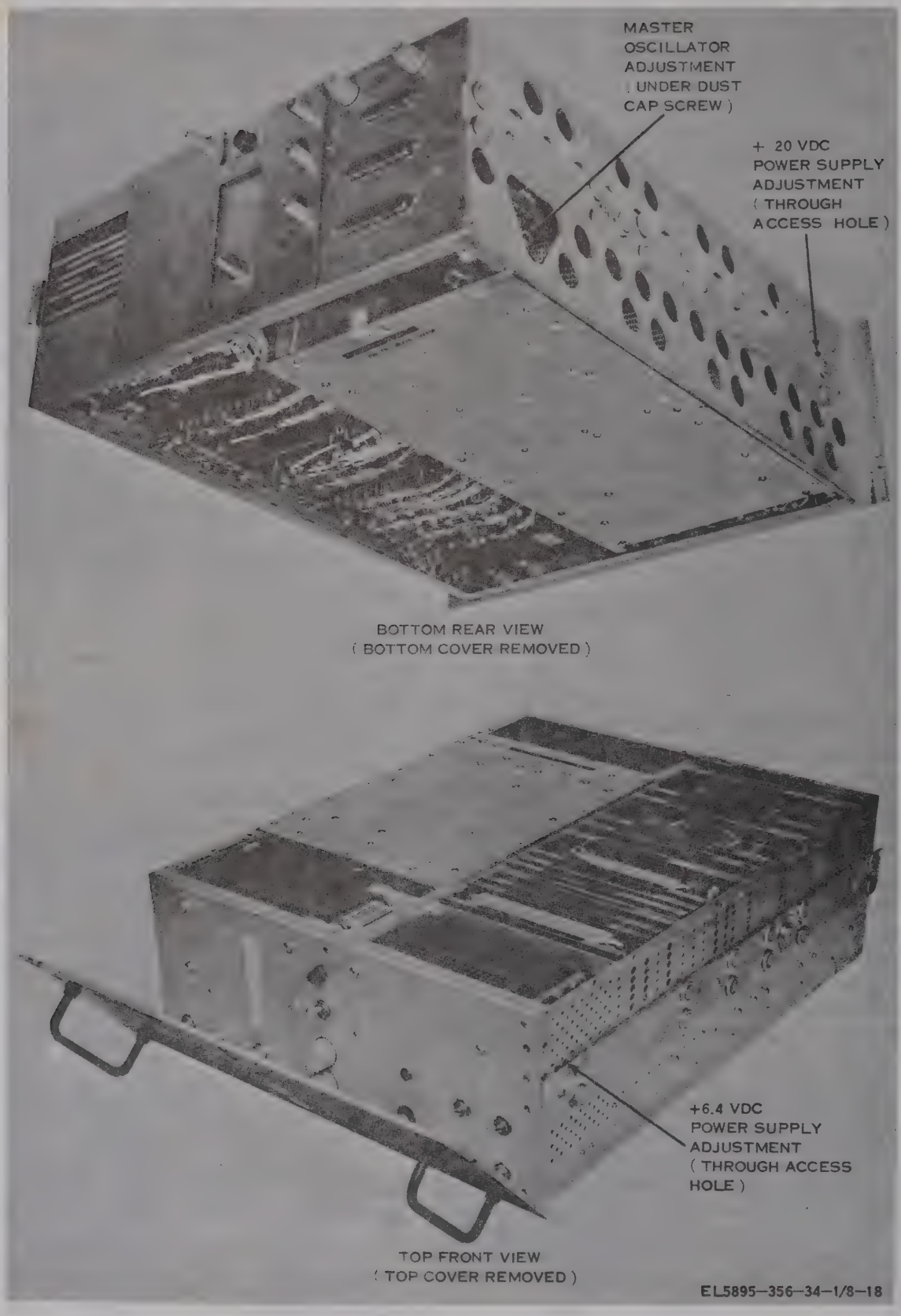


Figure 3-5. Transmitter adjustments.

Table 3-12. Printed Circuit Card Adjustments Card

PC card	Ref des No.	loc. code No.	Para ref 3-28	Location of adjustments
Dual balanced modulator Ch A1/B1	A7	17		
Filter pair Ch A1/B1	A3	16		
Dual balanced modulator Ch A2/B2	A21	17		
Filter pair Ch A2/B2	A6	15		
Multiplex carrier generator	A9	13		
Signal control	A5	9	c,g,h	See figure FO-8.
Transmit gain control	A4	8	e	See figure FO-9.
31-Pin extender	A20			
Frequency select memory	A13	7		
Frequency select memory	A14	7		
Frequency select memory	A15	7		
Band control	A16	6		
Code converter matrix No. 1	A17	5		
Code converter matrix No. 2	A18	4		
41-pin extender	A12			
Automatic channel loading	A8	18	f	See figure FO-10.

NOTE

Cards with same card location code numbers are interchangeable.

(8) Disconnect the test setup.

b. +20 Vdc Power Supply A11 Adjustment. This adjustment is performed with a differential voltmeter and 31-pin extender board A20.

(1) Insure transmitter POWER ON/OFF switch is OFF.

(2) Install signal control card A5 (fig. FO-51①) in the transmitter chassis using 31-pin extender card A20.

(3) Set the differential voltmeter to measure +20 Vdc.

(4) Connect a test cable between G(ground) on the digital voltmeter and the transmitter chassis.

(5) Connect a test cable between the positive jack of the differential voltmeter and pin A of signal control card A5.

(6) Set transmitter POWER ON/OFF switch to ON.

(7) Adjust +20 Vdc power supply adjustment (fig. 3-5) for +20 ±0.1 Vdc as indicated on the differential voltmeter.

(8) Disconnect the test setup.

c. Signal Control Card A5 −20 Vdc Adjustment. This adjustment is performed with a differential voltmeter and 31-pin extender board A20.

(1) Insure transmitter POWER ON/OFF switch is OFF.

(2) Install signal control card A5 (fig. FO-51①) in the chassis using 31-pin extender board A20.

(3) Set the digital voltmeter to measure −20 Vdc.

(4) Connect a test cable between G (ground) of the differential voltmeter and the transmitter chassis.

(5) Connect a test cable between the negative jack of the differential voltmeter and pin H of signal control card A5.

(6) Set transmitter POWER ON/OFF switch to ON.

(7) Adjust potentiometer R76 on signal control card A5 (table 3-12) for −20 ±0.1 Vdc as indicated on the differential voltmeter.

(8) Disconnect the test setup.

d. Frequency Synthesizer A2 5-MHz Clock Adjustment. This adjustment is performed with a digital electronic counter, a 20-db attenuator, and the test set.

NOTE

This adjustment is performed without removing the frequency synthesizer (A2) from the transmitter chassis. An opening in the left rear side of the transmitter chassis and frequency synthesizer side cover enables access to this adjustment (fig. 3-5). A screw type dust cover seals the 5-MHz clock

adjustment chassis opening. This dust cover must be removed to gain access to the adjustment.

(1) Insure the transmitter POWER ON/OFF switch is OFF.

(2) Connect a digital electronic counter and 20-db pad attenuator to transmitter output jack J1 as shown in figure 3–2.

(3) Set transmitter POWER ON/OFF switch to ON.

NOTE

Allow the transmitter a 1-hour warmup period before performing this alignment.

(4) Set the FREQUENCY SELECT thumbwheel switches on the test set to 29.9999 MHz.

(5) Set the PC switch and the KEY switch on the test set to ON.

(6) Depress the XMTR DTE pushbutton on the test set.

(7) Adjust the 5-MHz clock adjustment (fig. 3–5) for a stable 29.9999 MHz ±3 Hz indication on the digital electronic counter.

(8) Set PC switch and KEY switch on the test set to the down (off) position.

(9) Disconnect the test setup.

e. Transmit Gain Control (TGC) Card A4 Alignment. This adjustment is performed with the test set, the 31-pin extender board A20, a differential voltmeter, and multimeter.

(1) Insure transmitter POWER ON/OFF switch is OFF.

(2) Set transmitter EXCITER GAIN control to the full cw position.

(3) Set the transmitter CARRIER ADJUST LOCAL switch to STEP and the LOCAL STEP (−db) switch to 0.

(4) Set TGC ON/OFF switch (S1) on transmit gain control card A4 (table 3–12) to ON.

(5) Connect the transmitter front panel TGC VOLTAGE test point to the test set +0.75V jack (fig. 3–2).

(6) Install transmit gain control card A4 (table 3–12) in the transmitter using 31-pin extender card A20.

(7) Set the transmitter POWER ON/OFF switch to ON.

(8) Set the PC switch on the test set to ON.

(9) Connect a test cable between the TGC jack (−) on test set and the positive jack of the differential voltmeter.

(10) Adjust TGC control on test set for −7 ±0.1 Vdc.

(11) Connect a test cable between the positive jack of the differential voltmeter and test point TP10 on the transmit gain control card A4.

(12) Connect a test cable between the negative jack of the differential voltmeter and test point TP11 on the transmit gain control card A4.

(13) Adjust potentiometer R5 on transmit gain control card A4 (table 3–12) for 0 volt ±25 mv as indicated on the differential voltmeter.

(14) Remove the test connection from TP10 and connect it to test point TP1 on the transmit gain control card A4.

(15) Remove the test connection from TP11 and connect it to test point TP2 on the transmit gain control card A4.

(16) Adjust potentiometer R7 on the transmit gain control card A4 (table 3–12) for 0 volt as indicated on the differential voltmeter.

(17) Remove the test connection from TP2 and the negative jack of the differential voltmeter.

(18) Connect a test cable between the G (ground) jack of the differential voltmeter and the transmitter chassis ground.

(19) Adjust potentiometer R9 on the transmit gain control card A4 (table 3–12) for 3 volts as indicated on the differential voltmeter.

NOTE

There is interaction between potentiometer R7 and R9. If step (19) is not obtained, repeat steps (12) through (19) above until the desired results of step (19) are obtained.

(20) Remove the test connection from TP1 and connect it to test point TP9 on the transmit gain control card A4.

(21) Remove the +0.75 Vdc load from the transmitter TGC VOLTAGE test point.

(22) Connect the RF voltmeter to transmitter jack J1 as shown in figure 3–2.

(23) Adjust the TGC voltage control on the test set above and below the −7 Vdc setting while observing the RF voltmeter.

(24) The RF voltmeter will indicate a sweeping output above and below the −7 Vdc. Note the voltage level on the multimeter when the sweep indication on the RF voltmeter starts above and below the −7 Vdc. The difference between the voltage levels above and below the −7 Vdc when the sweeping action starts is the dead zone voltage (no change in the output level as indicated on the RF voltmeter). This voltage should be between −6.4 and −7.6 Vdc; a 1.2 Vdc difference.

(25) If the dead zone voltage is not 1.2 Vdc, adjust potentiometer R5 on the transmit gain control card A4 for the 1.2 Vdc difference level.

NOTE

It may be necessary to readjust R9 (step (19) above) slightly to keep the dead zone centered around −7 Vdc.

(26) Set the TGC control on the test set to full ccw and observe the RF voltmeter. A minimum sweep deflection of 18 db should be observed on the RF voltmeter.

(27) Disconnect the test setup.

f. Automatic Channel Loading Card A8 Adjustment. This adjustment is performed with the test set, the RF voltmeter, and a 20-db attenuator.

(1) Insure transmitter POWER ON/OFF switch is OFF.

(2) Connect the 20-db attenuator and the RF voltmeter as shown in figure 3–2.

(3) Set the transmitter POWER ON/OFF switch to ON.

(4) Set TUNE PWR switch on the test set to the up (on) position.

(5) Adjust potentiometer R14 (table 3–12) on automatic channel loading card A8 for 400 mv as indicated on the RF voltmeter.

NOTE

If 400 mv cannot be obtained by adjusting R14, adjust potentiometer R71 (table 3–12) on signal control card A5 to obtain the correct voltage level indicated in step (5) above.

(6) Disconnect the test setup.

g. Signal Control Card A5 AM Level Adjustment. This adjustment is performed with the test set, the RF voltmeter, and a multimeter.

(1) Insure transmitter POWER ON/OFF switch is OFF.

(2) Connect the 20-db attenuator and the RF voltmeter to transmitter output jack J1 as shown in figure 3–2.

(3) Connect a multimeter to the output of the test power supply and adjust the test power supply for a +0.75 Vdc output. Connect the test set +0.75V jack to the transmitter TGC VOLTAGE test point as shown in figure 3–2.

(4) Set the transmitter POWER ON/OFF switch to ON.

(5) Set the transmitter CARRIER ADJUST switch to AM.

(6) Select 29.9990 MHz on the test set FREQUENCY SELECT thumbwheel switches.

(7) Depress the XMTR DTE pushbutton on the test set.

(8) Ensure the AUDIO INPUT CH A2, CH A1, CH B1, and CH B2 toggle switches on the test set are set to the down position (off).

(9) Set KEY switch on the test set to the up position (on).

(10) Adjust potentiometer R66 on signal control card A5 (table 3–12) for a 225-mv reading on the RF voltmeter.

(11) Disconnect the test setup.

NOTE

Prior to performing any ALC alignment on signal control card A5 the following test procedure (steps (1) through (13)) should be performed first. This procedure determines whether alignment of the ALC is required or not.

h. Signal Control Card A5 ALC and TGC Alignment. This alignment procedure is performed with the test set, audio oscillator, a 31-pin extender board A20, a multimeter, a rms voltmeter (VTVM), a differential voltmeter, an oscilloscope, an ac VTVM, and a RF voltmeter.

(1) Insure the transmitter POWER ON/OFF switch is OFF.

(2) Insert signal control card A5 (fig. FO–51①) into the transmitter chassis jack using 31-pin extender board A20.

(3) Set transmitter POWER ON/OFF switch to ON.

(4) Set the RCVR XMTR NORMAL LEVELS switch on the test set to XMTR A1.

(5) Set the OSC switch on the test set to A1, and adjust the OSC LVL control for a reading of −6 db on the NORMAL LEVELS meter.

(6) Connect an ac VTVM to J306 pin U (signal control card A5).

NOTE

Insure ALC switch S1 (table 3–12) on signal control card A5 is set to ON and the voltage level at ALC test jack on the test set is 0V.

(7) Set AUDIO INPUT CH A1 toggle switch on the test set to up position (on)

(8) Adjust MODULATION LEVEL A1 control on the transmitter front panel for a 5 ±1 mVrms indication on the ac VTVM.

(9) Remove the ac VTVM test connection from J306 pin U and connect it to TP3 on the back of signal control card A5. The ac VTVM should indicate 150 ±25 mVrms.

(10) Connect a dc VTVM, set to measure a negative dc voltage, to the TGC test jack on the test set. Adjust the TGC voltage control on the test set for −9 Vdc as indicated on the dc VTVM.

(11) Note the reading in db on the ac VTVM connected to TP3.

(12) Remove the dc VTVM connection at the TGC test jack and connect a jumper cable between the TGC test jack and ALC test jack on the test set.

(13) The ac VTVM should indicate a 20 ±2 db reduction at TP3.

NOTE

If the indication of step (9) and/or (13) is not correct, proceed to step (14) below to correct the ALC range.

(14) Adjust potentiometer R39 (table 3–12) on signal control card A5 for a 5-db increase above that indicated on the ac VTVM (step (13)).

(15) Remove the jumper cable from the ALC test jack on the test set.

(16) Adjust potentiometer R10 (table 3–12) on signal control card A5 for 150 mv ±25 m Vrms as indicated on the ac VTVM; note the reading in db.

(17) Connect the jumper cable back into the ALC test jack on the test set. The ac VTVM should indicate a change of 20 ±2 db reduction at TP3.

(18) If step (17) above is incorrect, repeat steps (14) through (17) until the indicated results in steps (16) and (17) are obtained.

(19) Note the voltage level indicated on the VTVM; it should be 150 ±25 mVrms.

(20) Set ALC ON/OFF switch S1 (table 3–12) on signal control card A5 to OFF and adjust potentiometer R41 on A5 for an indication within 25 mv of the value noted in step (19) above. This completes the ALC amplifier alignment procedure.

(21) Set ALC ON/OFF switch S1 on the signal control card A5 (table 3–12) to ON.

(22) Insure that a jumper cable is connected from the +0.75 V test jack on the test set to the TGC VOLTAGE jack on the transmitter front panel.

(23) Connect a differential voltmeter to TP5 on the back of signal control card A5. Adjust A5 R26 (table 3–12) for a reading of 0.5 ±0.1 Vdc on the differential voltmeter.

(24) Disconnect the differential voltmeter from TP5 and connect it to TP4 on the back of signal control card A5. Adjust A5 R34 (table 3–12) for a reading of 2.5 ±0.1 Vdc on the differential voltmeter.

(25) Connect the oscilloscope and ac VTVM to TP6 on the back of signal control card A5. Adjust A5 R69 (table 3–12) approximately three turns from the fully clockwise position. Readjust A5 R26 (table 3–12) for a 50 mv p-p reading on the oscilloscope.

(26) Remove the +0.75 Vdc lead from the TGC VOLTAGE jack on the transmitter panel. Observe the db scale on the ac VTVM as the TGC dc output (at J306 pin *a*) sweeps from 0 to 4.0 Vdc. The total change in signal level should be between 8 and 13 db. If the TGC signal range is out of tolerance, perform steps (27) through (29) below to correct the TGC range.

(27) Reconnect the +0.75 Vdc lead to the TGC VOLTAGE jack on the transmitter front panel and adjust A5 R34 and A5 R26 (table 3–12) in small steps to achieve the 50 mv p-p operating level (as observed on the oscilloscope) and the 8 to 13 db TGC range required while sweeping.

(28) Remove oscilloscope and ac VTVM from TP6 of signal control card A5.

(29) Connect an RF voltmeter to the output of the 20db attenuator at transmitter J1 (fig. 3–2). Adjust A5 R69 (table 3–12) for a 0.75 Vrms level on the RF voltmeter. This completes the TGC amplifier alignment procedure.

(30) Perform the signal control card A5 am level adjustment procedure (*g* above).

(31) Perform the automatic channel loading card A8 adjustment procedure (*f* above).

3–29. Removal and Replacement Procedures

a. Transmitter Chassis (6A9 or 6A11).

(1) *Removal.* The transmitter is mounted on slide-type supporting tracks which facilitate withdrawing it from the electrical equipment rack unit 6. To remove the transmitter perform the following steps:

(*a*) Switch the transmitter POWER ON/OFF switch to OFF, and insure that power to the transmitter is removed.

(*b*) Remove four screws at sides of front panel which secure the drawer in the rack.

(*c*) Pull the drawer forward until it is fully extended.

(*d*) Disconnect the power and signal cables.

CAUTION

Support the drawer when separating it from the supporting tracks. The drawer weighs approximately 65 pounds.

(*e*) Depress levers on each side of supporting tracks and pull transmitter free from rack.

(2) *Disassembly.* Disassembly of the transmitter is a depot level function; however, in order to remove assemblies from within the transmitter, the top or bottom covers must first be removed. Refer to figure FO–51 for location of assemblies and printed circuit cards.

(3) *Reassembly.* Install top and bottom covers and front panel, and tighten mounting screws.

(4) *Replacement.* To replace the transmitter, perform the following steps:

CAUTION

To prevent cable cutting during transmitter installation, insure that cables are positioned so as not to be damaged when the drawer is pushed into the rack. When both transmitters are to be installed, push in bottom transmitter first.

(*a*) Align mounting bars on the sides of the transmitter with the slide devices and slide the transmitter inward until the stops reset.

(*b*) Connect power and signal cables.

CAUTION

To prevent accidental shorts, insure that top and bottom cover plates are installed when operating the transmitter in the pushed-in position in the rack.

(*c*) Push transmitter into rack and secure four mounting screws in the front panel.

(*d*) Set the transmitter POWER ON/OFF switch to the ON position.

(*e*) If the transmitter is new or has been readjusted, perform the rack-mounted transmitter performance test (para 3–31).

b. Printed Circuit (PC) Cards.

(1) *Removal.* The PC cards are held in place by edge guides and by the friction grip of the electrical connector. To remove a PC card, perform the following steps:

(*a*) Switch the transmitter POWER ON/OFF switch to OFF.

(*b*) Pull transmitter drawer out to fully-extended position and remove top cover.

(*c*) Remove the card extraction tool from the retaining clips (fig. FO–51①) and carefully insert the prongs of the extraction tool (fig 3–6) into the mating holes on the top edge of the PC card.

(*d*) Place one hand firmly against the top edge of the PC card in order to cushion the shock during card removal.

(*e*) With the other hand, pull gently but firmly to unseat the PC card from its connector.

CAUTION

Do not jerk the PC card out of the card basket assembly. Striking the components against adjacent cards may result in equipment failure.

(*f*) Remove the extraction tool from the PC card, then lift the PC card free from the card basket assembly.

(*g*) Replace the card extraction tool in the retaining clips.

(2) *Replacement.*

(*a*) Verify that transmitter power is off.

(*b*) Verify that the PC card about to be

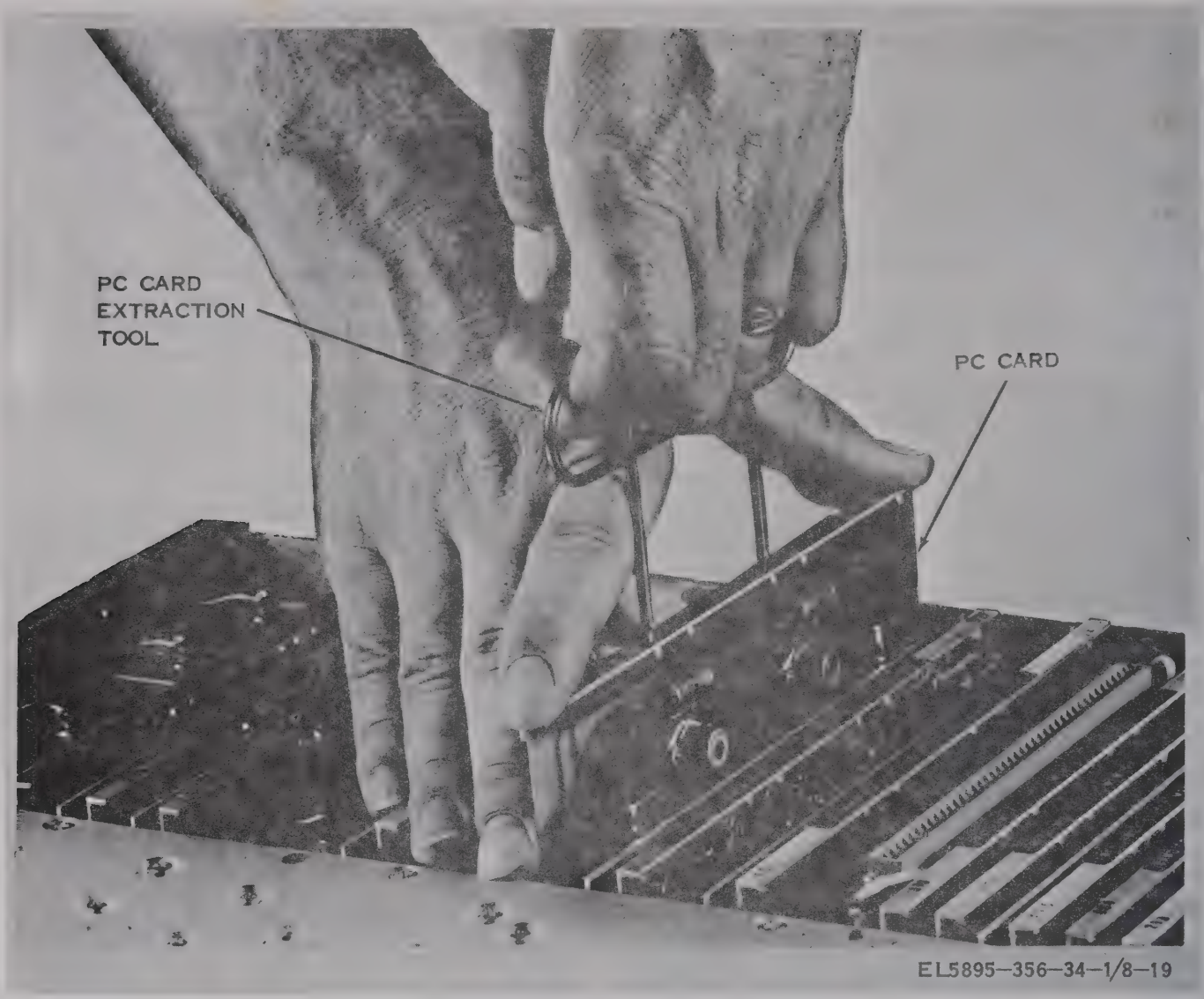


Figure 3-6. Printed circuit card removal with extraction tool.

installed is the proper type and that the location numbers match (table 3-12).

(*c*) Insert PC card into card guides and slide PC card until the card contacts touch the connector spring contacts.

(*d*) Using both thumbs, apply firm pressure evenly to each side of the top edge of the PC card. The top edge of the PC card will be in line with adjacent PC cards when properly seated.

CAUTION

Do not strike PC card to seat it. Rough handling may cause permanent damage to shock-sensitive components.

(*e*) If the PC card is new or repaired, perform the applicable adjustment or alignment procedure (table 3-11).

c. RF Translator Assembly (A1).

(1) *Removal.*

(*a*) Remove the receiver top cover plate.

(*b*) Remove the screws securing the RF translator to the center divider and to the side of the drawer (four screws per side).

(*c*) Lift out the assembly as necessary to disconnect the power and signal cables.

(*d*) Remove power connector plug P5405 by loosening the two attached screws. Grasp the power connector plug and pull it gently away from the RF translator (A1) assembly so that the power connector plug separates from the chassis jack J5405.

(*e*) Disconnect coaxial cable plugs, P5401 P5402, P5403 and P5404.

(*f*) Lift the RF translator (A1) assembly from the transmitter chassis drawer.

(2) *Replacement.* Replacement procedures for the RF translator (A1) assembly are the reverse of those for removal.

d. Frequency Synthesizer Assembly (A2).

(1) *Removal.*

(*a*) Remove the transmitter and remove the transmitter bottom cover plate (para 3-29*a*).

(*b*) Remove the six screws securing the synthesizer to the center divider and to the side of the drawer (fig. 3-7). Control the synthesizer carefully while removing the screws so that it does not fall.

(*c*) Lift the frequency synthesizer assem-

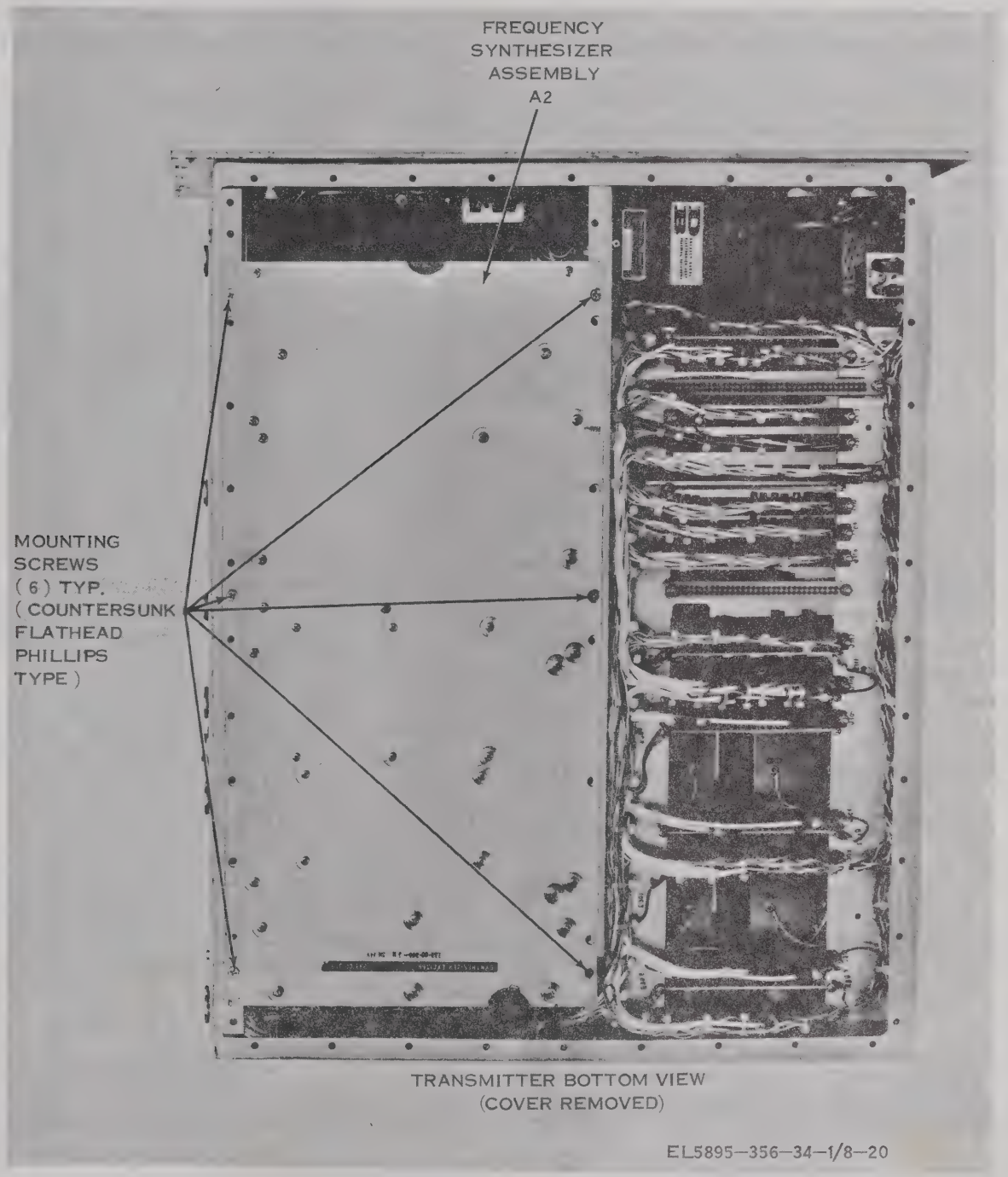


Figure 3-7. Frequency synthesizer A2 removal.

bly as necessary to disconnect the power and signal connectors.

(*d*) Remove the two attaching screws on power connector P3801 and disconnect the power connector.

(*e*) Disconnect coaxial cable plug connectors P3804, P3805, and P3807.

(*f*) Lift the frequency synthesizer assembly from the drawer.

(2) *Replacement.* Replacement procedures for the synthesizer assembly are the reverse of those for removal.

Section IV. DIRECT SUPPORT TESTING

3-30. General

This section provides both rack-mounted and bench performance tests for transmitter assemblies repaired at direct support level. Each performance test verifies that repaired equipment is functioning in accordance with specific performance standards before it is returned to the using organization. These testing procedures may also be used as a guide for troubleshooting. Refer to the applicable troubleshooting charts in section II when performance standards are not met.

3-31. Rack-Mounted Transmitter Performance Test

a. General. This test checks the overall performance of each of the two transmitters (6A9 or 6A11) while they are mounted in their normal operating positions in the shelter. The test should be performed step-by-step noting what the required operation is before proceeding to the next step. If the required indications are not observed, perform troubleshooting procedures in section II of this chapter. The following test procedures (performance tests) are provided:

Table 3-13. Frequency Tuning Range, Performance Standard Test
Table 3-14. Power Output, Performance Standard Test
Table 3-15. Automatic Load Control (ALC), Performance Standard Test
Table 3-16. Front Panel Control, Performance Standard Test
Table 3-17. Transmit Gain Control, Performance Standard Test

b. Test Equipment and Materials. The following test equipment and materials are required to perform this test procedure:

(1) RF voltmeter AN/URM-145, with 50-ohm adapter probe (Boonton 91-8B).

(2) 20-db fixed attenuator 8491A HP.

(3) Signal Generator (audio oscillator) AN/URM-127.

(4) Digital Electronic Counter AN/USM-207.

(5) Power Supply PP-2309/U (2 each).

c. Test Connections and Conditions. This test shall be performed with the transmitters mounted in their respective rack positions. All equipment should be operating for a minimum time of 1 hour before commencing the test. The RF patch panel (6A6) and either one of the two transmitters (6A9, 6A11) are used as shown in figure 3-1 to perform this test. The output from the transmitter should, in turn, be connected through the RF patch panel to the applicable test equipment.

CAUTION

To prevent permanent damage to the transmitter, insure that a 20-db fixed attenuator is connected to the RF patch panel (6A6) PRIM EXCITER/SEC EXCITER jack.

(1) Energize the radio subsystem in accordance with procedures in TM 11-5895-356-12-1, except for 10-kw (unit 2) and 1-kw (unit 6A8) linear power amplifiers.

CAUTION

Testing is accomplished using the transmitter only. Insure that the two linear power amplifiers (unit 2, and unit 6A8) are deenergized by setting the following switches in their off positions.

Unit	*Switch*	*Position*
1A3	PRI LIN PWR AMP	down
1A2	SEC LIN PA	down
6A8	POWER ON/OFF	OFF
2	FIL ON/OFF	OFF
2	HV ON/OFF	OFF

(2) Set the transmitter controls as listed below.

Control/indicator	*Setting*
EXCITER GAIN control	10
CARRIER ADJUST–LOCAL switch.	REMOTE
CARRIER ADJUST–LOCAL STEP (−db) switch.	0
TGC ON/OFF switch	OFF (see table 3–12)
ALC ON/OFF switch	ON (see table 3–12)
TGC VOLTAGE jack	Apply +0.75 ±0.05 Vdc
POWER ON/OFF switch	ON

d. Initial Test Equipment Settings. Test equipment control settings are included in the control settings column of the performance standard tests.

Table 3–18. Frequency Tuning Range, Performance Standard Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	Digital electronic counter, 20-db attenuator.		At RF patch panel (6A6) connect a 20-db attenuator to the PRIM EXCITER/SEC EXCITER jack. Connect a test cable between the other connector on the 20-db attenuator and the INPUT to a digital electronic counter.	
2			At mode and status panel (7A5/7A12) set KEY LINE switch to XMIT, XMTR PLT CARR to position 3, NORMAL LEVEL SEL switch to EXCITER RF, and RF PWR SEL switch to FWD.	At mode and status panel (7A5/7A12) NORMAL LEVELS meter indicates in the green dial area.
3			At frequency select panel (7A4/7A11) select the frequency listed in step 4 below in turn on the TRANSMITTER FREQUENCY SELECT thumbwheel switches, depress the XMTR TUNE pushbutton after each frequency is selected and observe the following: *a.* The XMTR TUNE pushbutton illuminates for less than 10 seconds after it is depressed. *b.* The TRANSMITTER FREQUENCY DISPLAY on 7A4/7A11 indicates the frequency selected. *c.* The digital electronic counter indicates the frequency selected ±3 Hz.	
4			TRANSMITTER FREQUENCY SELECT MEGA-CYCLES thumbwheel switch settings on frequency select panel (7A4/7A11): 2.0000 MHz 2.1990 MHz 2.2000 MHz 2.4990 MHz 2.5000 MHz	TRANSMITTER FREQUENCY DISPLAY on frequency select panel (7A4/7A11) indicates and the digital electronic counter indicates within ±3 Hz. 2.0000 MHz 2.1990 MHz 2.2000 MHz 2.4990 MHz 2.5000 MHz

		2.8990 MHz	2.8990 MHz
		2.9000 MHz	2.9000 MHz
		3.1111 MHz	3.1111 MHz
		3.3990 MHz	3.3990 MHz
		3.4000 MHz	3.4000 MHz
		3.9990 MHz	3.9990 MHz
		4.0000 MHz	4.0000 MHz
		4.2222 MHz	4.2222 MHz
		4.7990 MHz	4.7990 MHz
		4.8000 MHz	4.8000 MHz
		5.7990 MHz	5.7990 MHz
		5.8000 MHz	5.8000 MHz
		6.9990 MHz	6.9990 MHz
		7.0000 MHz	7.0000 MHz
		7.3333 MHz	7.3333 MHz
		10.4444 MHz	10.4444 MHz
		11.9990 MHz	11.9990 MHz
		12.0000 MHz	12.0000 MHz
		15.5555 MHz	15.5555 MHz
		16.9990 MHz	16.9990 MHz
		17.0000 MHz	17.0000 MHz
		18.6666 MHz	18.6666 MHz
		21.7777 MHz	21.7777 MHz
		21.9990 MHz	21.9990 MHz
		22.0000 MHz	22.0000 MHz
		26.8888 MHz	26.8888 MHz
		26.9990 MHz	26.9990 MHz
		27.0000 MHz	27.0000 MHz
		29.9990 MHz	29.9990 MHz
		29.9999 MHz	29.9999 MHz

Table 3–14. Power Output, Performance Standard Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1			At frequency select panel unit (7A4/7A11) select 29.9990 MHz on TRANSMITTER FREQUENCY SELECT MEGACYCLES thumbwheel switches and depress the XMTR TUNE pushbutton.	XMTR TUNE pushbutton lamp illuminates for less than 10 seconds and TRANSMITTER FREQUENCY DISPLAY on 7A4/7A11 indicates 29.9990.
2			At mode and status panel unit (7A5/7A12) set XMTR CHAN B1, CHAN A1, and CHAN A2 pushbutton switches to off and CHAN B2 to on.	STATUS TRANSMITTER CH A2, CH A1, and CH B1 indicator lamps are extinguished and CH B2 is illuminated. CHAN A2, CHAN A1, and CHAN B1

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
				pushbutton lamps are extinguished and CHAN B2 pushbutton lamp is illuminated.
3			Connect the output of an audio oscillator to the SEND B2 PRIMARY RADIO/SECONDARY RADIO jack on audio patch panel 7A15. Set the output of the audio oscillator to 1 kHz.	
4			On mode and status panel (7A5/7A12) set NORMAL LEVEL SEL switch to EXCITER AUDIO.	
5			Set NORMAL LEVEL AUDIO SEL switch on 7A5/7A12 to B2.	NORMAL LEVELS meter on 7A5/7A12 indicates a signal level.
6			Adjust the output GAIN of the audio oscillator for a NORMAL LEVELS meter indication at the crossover point of the red and green scales on 7A5/7A12.	NORMAL LEVELS meter on 7A5/7A12 indicates in the red and green area crossover point.
7			At RF patch panel (6A6) connect a 20-db attenuator to PRIM EXCITER/SEC EXCITER jack. Connect a test cable between the other connector on the 20-db attenuator and the 50-ohm probe on an RF voltmeter.	
8			On mode and status panel (7A5/7A12) set KEY LINE switch to XMIT. *Note.* Adjust MODULATION LEVEL B2 control on the transmitter (6A9/6A11) to obtain a signal level in step 8 if required.	RF voltmeter indicates a signal level output.
9			At audio patch panel (7A15) remove the audio test connector from the PRIMARY RADIO/SECONDARY RADIO SEND B2 jack and connect it to the PRIMARY RADIO/SECONDARY RADIO SEND B1 jack.	
10			At the mode and status panel (7A5/7A12) set NORMAL	NORMAL LEVELS meter on 7A5/7A12 indicates in the red

			LEVEL AUDIO SEL switch to B1, XMTR CHAN B1 pushbutton switch on, and XMTR CHAN B2 off.	and green area crossover point, XMTR CHAN B1 pushbutton switch illuminates, and CHAN B2 is extinguished. STATUS TRANSMITTER CH B1 indicator is illuminated and CH B2 is extinguished. RF voltmeter indicates signal level output.
			Note. Adjust MODULATION LEVEL B1 control on the transmitter (6A9/6A11) to obtain a signal level on the RF voltmeter as required.	
11			At the audio patch panel (7A15) remove the audio test connection from the PRIMARY RADIO/SECONDARY RADIO SEND B1 jack and connect it to the PRIMARY RADIO/SECONDARY RADIO SEND A1 jack.	
12			At the mode and status panel (7A5/7A12) set NORMAL LEVEL AUDIO SEL switch to A1, XMTR CHAN A1 pushbutton switch on, and XMTR CHAN B1 off. *Note.* Adjust MODULATION LEVEL A1 control on the transmitter (6A9/6A11) to obtain a signal level on the RF voltmeter as required.	NORMAL LEVELS meter on 7A5/7A12 indicates in the red and green area crossover point. XMTR CHAN A1 pushbutton switch illuminates and CHAN B1 is extinguished. STATUS TRANSMITTER CH A1 indicator is illuminated and CH B1 is extinguished. STATUS TRANSMITTER CH A1 is extinguished. RF voltmeter indicates a signal level output.
13			At the audio patch panel (7A15) remove the audio test connection from the PRIMARY RADIO/SECONDARY RADIO SEND A1 jack and connect it to the PRIMARY RADIO/SECONDARY RADIO SEND A2 jack.	
14			At the mode and status panel (7A5/7A12) set NORMAL LEVEL AUDIO SEL switch to A2, XMTR CHAN A2 pushbutton switch on and XMTR CHAN A1 off. *Note.* Adjust MODULATION LEVEL A1 control on the trans-	NORMAL LEVELS meter on 7A5/7A12 indicates in the red and green crossover point. XMTR CHAN A2 pushbutton switch illuminates and CHAN A1 is extinguished. STATUS TRANSMITTER CH A2 indicator is illuminated and CH A1 is

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
			mitter (6A9/6A11) to obtain a signal level on the rf voltmeter as required.	extinguished. RF voltmeter indicates a signal level output.

Table 3–15. Automatic Load Control (ALC), Performance Standard Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	RF voltmeter, 20-db attenuator		At RF patch panel 6A6, connect a 20-db attenuator to the PRIM EXCITER/SEC EXCITER jack. Connect the 50-ohm probe of an RF voltmeter to the other connector of the 20-db attenuator.	
2		Set ALC ON/OFF switch S1 (table 3–12) on signal control card A5 to ON.		
3			At the frequency select panel (7A4/7A11) select 29.9990 on the TRANSMITTER FREQUENCY SELECT MEGACYCLES thumbwheel switches and depress the XMTR TUNE pushbutton.	TRANSMITTER FREQUENCY DISPLAY on the frequency select panel (7A4/7A11) indicates 29.9990 and XMTR TUNE pushbutton illuminates for less than 10 seconds.
4	Audio oscillator set to 1-kHz output		Connect the output of the audio oscillator to the PRIMARY RADIO/SECONDARY RADIO SEND A1 jack at audio patch panel 7A15.	
5			Depress XMTR CHAN A1 pushbutton on the mode and status panel (7A5/7A12) to on.	XMTR CHAN A1 pushbutton switch illuminates and STATUS TRANSMITTER CH A1 illuminates on the mode and status panel (7A5/7A12).
6			Set NORMAL LEVEL SEL switch on the mode and status panel (7A5/7A12) to EXCITER AUDIO and set NORMAL LEVEL AUDIO SEL switch to A1.	
7	Audio oscillator OUTPUT GAIN adjust.		Adjust the OUTPUT GAIN adjust on the audio oscillator for a	NORMAL LEVELS meter on the mode and status panel (7A5/

			NORMAL LEVELS meter indication at the crossover point on the red and green scales on 7A5/7A12.	7A12) indicates in the red and green area crossover point.
8			Apply −0.75 Vdc to the transmitter TGC VOLTAGE test jack (TP 301).	
9			Set KEY LINE switch on the mode and status panel (7A5/7A12) to XMIT. *Note.* A slight adjustment of the transmitter EXCITER GAIN control may be required to obtain the correct performance standard.	RF voltmeter indicates 450 mv.
10			Apply −9 Vdc to PRI/SEC ALC test jack on the RF patch panel (6A6).	RF voltmeter indicates 18-db minimum reduction.

Table 3–16. Front Panel Controls, Performance Standard Test

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
1	RF voltmeter, 20-db attenuator		At the RF patch panel (6A6) connect a 20-db attenuator to the PRIM EXCITER/SEC EXCITER jack. Connect the 50-ohm probe of an RF voltmeter to the other connector of the 20-db attenuator.	
2	Test power supply		Apply 0.75 Vdc to the transmitter TGC VOLTAGE test point (TP 301).	
3			At the transmitter front panel (6A9/6A11), set CARRIER ADJUST LOCAL switch to STEP and the LOCAL STEP (−db) switch to 0. *Note.* If the test is being performed at the secondary mode and status panel, (7A5/7A12), set XMTR PLT CARR switch to 1.	Observe the RF voltmeter indication in db.
4			Rotate the LOCAL STEP (−db) switch on the transmitter cw to the first switch position.	The RF voltmeter indicates a decrease of 3 ±2 db below that of step 3.

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
5			Continue to rotate the LOCAL STEP (−db) switch on the transmitter cw to each of the switch settings through 30.	The RF voltmeter indicates a decrease of 3 ±2 db at each of the switch settings. At switch setting 30, the rf voltmeter should indicate a decrease of at least 30 db below that observed in step 3.
6			At the transmitter (6A9/6A11), set the CARRIER ADJUST LOCAL switch to CONT. Adjust the CARRIER ADJUST CONT. control to the maximum cw position.	The RF voltmeter indicates a minimum of 450 mv. Observe this indication in db.
7			Adjust the CARRIER ADJUST CONT. control on the transmitter (6A9/6A11) to the maximum ccw position.	The RF voltmeter should indicate a decrease of 30 db below that of step 6 (450 mv).
8			Set the CARRIER ADJUST LOCAL switch on the transmitter (6A9/6A11) to AM. *Note.* Adjust potentiometer R66 (table 3–12) on signal control card A5 as required for the correct performance standard indication.	The RF voltmeter should indicate 225 mv.
9			Set transmitter CARRIER ADJUST LOCAL switch to REMOTE. At the mode and status panel (7A5/7A12) set KEY LINE switch to PTT.	
10			At the frequency select panel (7A4/7A11) depress the XMTR TUNE pushbutton.	The RF voltmeter should indicate 200 ±50 mv.

Table 3–17. Transmit Gain Control (TGC), Performance Standard Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	RF voltmeter, 20-db attenuator		At the RF patch panel (6A6) connect a 20-db attenuator to the PRIM EXCITER/SEC EXCITER jack. Connect the 50-ohm probe of an RF voltmeter	

			to the other connector of the 20-db attenuator.	
2	Audio oscillator set to a 1-kHz output		Connect the output of the audio oscillator to the PRIMARY RADIO/SECONDARY RADIO A1 jack at the audio patch panel (7A15).	
3			Depress XMTR CHAN A1 pushbutton on the mode and status panel (7A5/7A12) to on.	XMTR CHAN A1 pushbutton switch illuminates and STATUS TRANSMITTER CH A1 illuminates on the mode and status panel (7A5/7A12).
4			At the mode and status panel (7A5/7A12) set NORMAL LEVEL SEL switch to EXCITER AUDIO and NORMAL LEVEL AUDIO SEL switch to A1.	
5	Audio oscillator OUTPUT GAIN adjust.		Adjust the OUTPUT GAIN of the audio oscillator for a NORMAL LEVELS meter indication at the crossover point on the red and green scales on 7A5/7A12.	NORMAL LEVELS meter on the mode and status panel (7A5/7A12) indicates in the red and green area crossover point.
6			Apply −0.5 Vdc to the transmitter TGC VOLTAGE test point (TP 301).	
7			At the mode and status panel (7A5/7A12) set KEY LINE switch to XMIT. *Note.* Adjust MODULATION LEVEL A1 control on the transmitter (6A9/6A11) to obtain the correct performance standard as required.	RF voltmeter indicates 450 mv.
8			At the mode and status panel (7A5/7A12) set KEY LINE switch to OFF and depress XMTR CHAN A1 pushbutton.	XMTR CHAN A1 pushbutton lamp extinguishes, STATUS TRANSMITTER CH A1 indicator lamp extinguishes, and RF voltmeter drops to a zero output.
9			At the mode and status panel (7A5/7A12) set XMTR PLT CARR switch to OFF, XMTR CHAN A1 depressed to on, and KEY LINE switch to TEST.	RF voltmeter indicates 450 mv.

Step No.	Control settings		Test procedure	Performance standard
	Test equipment	Equipment under test		
10			Remove the 0.5 Vdc from the transmitter TGC VOLTAGE test point (TP 301) and remove the −7 Vdc voltage from the PRI/SEC TGC test jack on the RF patch panel (6A6).	The RF voltmeter indicates a sweeping output varying over a minimum range of 18 db.
11			Apply −7 Vdc to the PRI/SEC TGC test point on the RF patch panel (6A6).	The RF voltmeter should stop sweeping. RF voltmeter indicates 450 mv.

3-32. Bench Transmitter Performance Test

a. General. The purpose of this test is to verify that the transmitter is in proper alignment and functioning within specified tolerances. Perform the test procedures in the sequence given, noting the required observation before proceeding to the next step. All switch settings referred to in this section are located on the receiver-transmitter test set front panel unless otherwise specified. All pushbuttons are momentarily depressed unless otherwise specified. If the required indications are not observed, perform troubleshooting procedures in section II of this chapter. The following test procedures (performance tests) are provided:

Table 3-18. Power Output Adjustment, Bench Performance Test

Table 3-19. Frequency Tuning Range, Bench Performance Test

Table 3-20. Automatic Load Control (ALC), Bench Performance Test

Table 3-21. Automatic Channel Loading, Bench Performance Test

Table 3-22. Transmit Gain Control, Bench Performance Test

Table 3-23. Front Panel Controls, Bench Performance Test

Table 3-24. Frequency Synthesizer, Bench Performance Test

b. Test Equipment and Materials. The following test equipment is required for the performance of the bench transmitter performance tests. All equipment shall be in current calibration. Similar equipment may be utilized if it is equivalent in performance.

Receiver-transmitter test set	Raytheon part No. T324732A
RF signal generator	AN/USM-44A
RF voltmeter	AN/USM-145
Frequency counter	AN/USM-207
Oscilloscope	AN/USM-281
VTVM	ME-303/U
VOM	AN/USM-210
Differential voltmeter	ME-202/U
50-ohm adapter	Boonton 91-8B

c. Documents. The following documents are required for reference: Operation and Maintenance Manual, Receiver-Transmitter Test Set (Raytheon Part No. T324732A).

d. Test Connections and Conditions. Perform the bench setup procedure of paragraph 3-24*b* and allow 1-hour warmup period before starting performance test procedure.

e. Initial Test Equipment Settings. Test equipment control settings are included in the control settings column of each test procedure.

Table 3-18. Power Output Adjustment, Bench Performance Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	See para 3-32. Frequency counter connected as shown in fig. 3-2.	See para 3-32	Set FREQUENCY SELECT thumbwheel switches on test set to 29.9990. Depress the XMTR DTE pushbutton on the test set.	XMTR DTE pushbutton illuminates less than 10 seconds. Frequency counter indicates 29.9990 MHz.
2			On the test set, set the RCVR XMTR NORMAL LEVELS switch to XMTR A1 position. Set the OSC switch to A1 and adjust OXC LVL control for a NORMAL LEVELS meter reading of 0 db.	
3	RF voltmeter set to measure 200 mVrms.		Disconnect the frequency counter and connect RF voltmeter as shown in fig. 3-2. Set AUDIO INPUT CH A1 toggle switch on the test set to ON. Set PC switch on the test set to the down (off) position.	
4			Adjust MODULATION LEVEL A1 potentiometer on the transmitter front panel (6A9/6A11). Set KEY switch on the test set to the down (off) position.	200-mv indication on the RF voltmeter.
5			Set AUDIO INPUT CH A1 toggle switch on the test set to the down (off) position. Set the OSC switch on the test set to A2 and set the KEY switch on the test set to the up (on) position.	
6	RF voltmeter (see step 3)		Set AUDIO INPUT CH A2 toggle switch on the test set to ON. Adjust MODULATION LEVEL A2 potentiometer on the transmitter front panel (6A9/6A11). Set KEY switch on the test set to the down (off) position.	200-mv indication on RF voltmeter.
7			Set AUDIO INPUT CH A2 toggle switch on the test set to the down (off) position. Set the OSC switch on the test set to B1. Set KEY switch on the test set to the up (on) position.	

8	RF voltmeter (see step 3)		Set AUDIO INPUT CH B1 toggle switch on the test set to ON. Adjust MODULATION LEVEL B1 potentiometer on the transmitter front panel. Set KEY switch on the test set to the down (off) position.	200-mv indication on RF voltmeter.
9			Set AUDIO INPUT CH B1 toggle switch on the test set to the down (off) position. Set the OSC switch on the test set to B2. Set KEY switch on the test set to the up (on) position.	
10	RF voltmeter (see step 4)		Set AUDIO INPUT CH B2 toggle switch on the test set to ON. Adjust MODULATION LEVEL B2 potentiometer on the transmitter front panel. Set KEY switch on the test set to the down (off) position.	200-mv indication on RF voltmeter.

Table 3–19. Frequency Tuning Range, Bench Peformance Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	See para 3–32. Set the following controls on the test set: *a.* KEY switch up. *b.* PC switch ON. *c.* RCVR XMTR switch to PWR. *d.* PC LVL potentiometer adjusted for a midscale reading on the NORMAL LEVELS meter.	See para 3–32	Disconnect the RF voltmeter from the test setup and connect the digital electronic counter as shown in fig. 3–2. Select the frequencies listed in step 2 in turn, on the test set FREQUENCY SELECT thumbwheel switches, depress the XMTR DTE pushbutton.	XMTR DTE lamp on the test set illuminates for less than 10 seconds and the frequency counter indicates the frequency selected within ±3 Hz.
2	Test set FREQUENCY SELECT thumbwheel switches:			Frequency counter indications:
	2.0000 MHz			2.0000 MHz
	2.1990 MHz			2.1990 MHz
	2.2000 MHz			2.2000 MHz
	2.4990 MHz			2.4990 MHz
	2.5000 MHz			2.5000 MHz
	2.8990 MHz			2.8990 MHz
	2.9000 MHz			2.9000 MHz
	3.1111 MHz			3.1111 MHz

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
	3.3990 MHz			3.3990 MHz
	3.4000 MHz			3.4000 MHz
	3.9990 MHz			3.9990 MHz
	4.0000 MHz			4.0000 MHz
	4.2222 MHz			4.2222 MHz
	4.7990 MHz			4.7990 MHz
	4.8000 MHz			4.8000 MHz
	5.7990 MHz			5.7990 MHz
	5.8000 MHz			5.8000 MHz
	6.9990 MHz			6.9990 MHz
	7.0000 MHz			7.0000 MHz
	7.3333 MHz			7.3333 MHz
	10.4444 MHz			10.4444 MHz
	11.9990 MHz			11.9990 MHz
	12.0000 MHz			12.0000 MHz
	15.5555 MHz			15.5555 MHz
	16.9990 MHz			16.9990 MHz
	17.0000 MHz			17.0000 MHz
	18.6666 MHz			18.6666 MHz
	21.7777 MHz			21.7777 MHz
	21.9990 MHz			21.9990 MHz
	22.0000 MHz			22.0000 MHz
	26.8888 MHz			26.8888 MHz
	26.9990 MHz			26.9990 MHz
	27.0000 MHz			27.0000 MHz
	29.9990 MHz			29.9990 MHz
	29.9999 MHz			29.9999 MHz
				Note. If frequency selection errors occur, the problem can be related to a particular frequency increment. If a frequency error is consistently related to a given increment, the fault can be related to a specific logic module or modules. See bench troubleshooting chart, step 5.

Table 3–20. Automatic Load Control (ALC), Bench Performance Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	See para 3–32.	See para 3–32	Disconnect the frequency counter and connect the RF voltmeter as shown in fig. 3–2.	

	RF voltmeter set to measure 450 mv rms. Test set PC switch to down. FREQUENCY SELECT thumbwheel switches set to 29.9990 MHz.	Set ALC ON/OFF switch (table 3–12) on signal control card A5 to ON.	Depress the XMTR DTE pushbutton on the test set.	XMTR DTE pushbutton lamp illuminates for less than 10 seconds.
2	RF voltmeter set to measure 450 mv.		Set the OSC switch on the test set to A1. Set RCVR XMTR NORMAL LEVELS switch to XMTR A1 and adjust OSC LVL control for −6-db level on NORMAL LEVELS meter. Set the AUDIO INPUT CH A1 switch on the test set to ON. Insure +0.75 Vdc is applied from the test set jack to the TGC VOLTAGE jack on the transmitter front panel.	RF voltmeter indicates 450 mv.
	RF voltmeter set to measure 450 mv.		*Note.* A slight adjustment of the transmitter EXCITER GAIN control may be required to correct standard.	RF voltmeter indicates 450 mv.
3			Connect a test cable between the TGC and ALC test jacks on the test set.	
4	Multimeter set to measure −9 Vdc.		Connect the multimeter to measure a negative voltage at either the TGC or ALC test jacks on the test set.	
5			Adjust the TGC potentiometer on the test set for −9 Vdc as indicated on the multimeter.	
6			At the test set: Set KEY switch to down. Set AUDIO INPUT CH A1 switch to down.	RF voltmeter indicates an 18-db minimum change.
7			Remove the test cable connected between the TGC and ALC test jacks.	

Table 3-21. Automatic Channel Loading, Bench Performance Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	See para 3-32. Set the test set KEY switch up, AUDIO INPUT CH A1 switch ON. Set the RF voltmeter to measure 450 mv.	See para 3-32.	Adjust the variable dc voltage applied to the transmitter TGC VOLTAGE test point.	316 mv as indicated on the RF voltmeter. Observe this level in db on the RF voltmeter.
2	----------	----------	Set the AUDIO INPUT CH B1 switch on the test set to ON.	The indication on the RF voltmeter should decrease by 2.7 db ±0.4 db from that of step 1.
3	----------	----------	Set the AUDIO INPUT CH A2 switch on the test set to ON.	The indication on the RF voltmeter should decrease by 4.7 db ±0.4 db from that of step 1.
4	----------	----------	Set the AUDIO INPUT CH B2 switch on the test set to ON. Set KEY switch to its down position and set the AUDIO INPUT CH A1, CH A2, CH B1, and CH B2 to their down positions.	The indication on the RF voltmeter should decrease by 6 db ±0.4 db from that of step 1.

Table 3-22. Transmit Gain Control, Bench Performance Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	See para 3-32 ----------	See para 3-32 ----------	Connect the test set +0.75 V jack to the transmitter TGC VOLTAGE test point on the transmitter front panel. *Note.* Use a multimeter to measure the above voltage. Set the OSC switch on the test set to A1.	
	Set the KEY switch up and the AUDIO INPUT CH A1 to ON at the test set.			
2	----------	----------	Adjust MODULATION LEVEL A1 potentiometer on the transmitter front panel.	450 mv as indicated on the RF voltmeter.
3	----------	----------	Set the KEY switch and the AUDIO INPUT CH A1 switch on the test set to the down position and insure the TGC ON/OFF switch (table 3-12) transmit gain on control card A5 to OFF.	

			Connect a multimeter set to measure a negative voltage to the TGC test jack on the test set. Adjust the TGC potentiometer on the test set for −7 Vdc as indicated on the multimeter.	
	Set the KEY switch up and the AUDIO INPUT CH A1 to ON at the test set.	At the transmitter, set the CARRIER ADJUST LOCAL to STEP, the STEP (−db) to 0, and the TGC ON/OFF switch to ON.		450 mv as indicated on the RF voltmeter.
4	----------	----------	Note the reading in db on the RF voltmeter and remove the +0.75 Vdc lead from the TGC VOLTAGE test point on the transmitter front panel. Adjust the TGC potentiometer on the test set to the maximum ccw position.	The RF output should sweep over a minimum range of 18 db as indicated on the RF voltmeter.
			Readjust the TGC potentiometer on the test set for a −7 Vdc multimeter indication.	The RF output should stop sweeping.
5	Set the KEY switch to down and the AUDIO INPUT CH A1 to down at the test set.	----------	Reapply the +0.75 Vdc test set voltage to the TGC VOLTAGE test point on the transmitter front panel.	RF voltmeter indicates 450 mv.

Table 3–23. Front Panel Controls, Bench Performance Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	See para 3–32 ----------	See para 3–32 ----------	Insure that the test set +0.75 V jack is connected to the transmitter TGC VOLTAGE test point.	
	At the test set insure that the KEY switch is down and AUDIO INPUT CH A1 is down.			
	Set the FREQUENCY SELECT thumbwheel switches to 29.9999 MHz at the test set.	----------	Depress the XMTR DTE pushbutton on the test set.	XMTR DTE pushbutton lamp illuminates for less than 10 seconds.
		Set the transmitter CARRIER ADJUST LOCAL switch to REMOTE.		
2	Set the PC switch to ON and the KEY switch to ON at the test set.	----------	Adjust PC LVL control on the test set to 450 mv as indicated on RF voltmeter.	

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
3			Adjust PC LEV control on the test set to 30 db below 450 mv as indicated on RF voltmeter.	
4	At the transmitter set the CARRIER ADJUST LOCAL switch to STEP and the STEP (−db) switch to 0.		Adjust EXCITER GAIN on the transmitter front panel as required for 450 mv as indicated on RF voltmeter (note this indication in db).	
5			Rotate the STEP (−db) switch on the transmitter cw to the first position.	The output should decrease 3 ±2 dB below 450 mv as indicated on the RF voltmeter.
6			Continue to rotate the STEP (−db) switch on the transmitter cw to each of its positions.	The output should decrease 3 ±2 db at each switch setting as indicated on the RF voltmeter.
7			At the maximum cw position (30), of the STEP (−db) switch the output should be 30 ±2 db below 450 mv as indicated on the RF voltmeter.	
8		At the transmitter front panel set the CARRIER ADJUST LOCAL switch set to CONT.	Adjust the CONT. potentiometer on the transmitter to the maximum cw position.	A minimum of 450 mv as indicated on the RF voltmeter (note this indication in db).
9			Adjust the CONT. potentiometer on the transmitter to the maximum ccw position.	The RF voltmeter should indicate a minimum change of 30 db below that of step 8.
10	Set the PC switch down at the test set	At the transmitter, set the CARRIER ADJUST LOCAL switch set to AM.	Adjust potentiometer R66 (table 3–12) on signal control card A5 as required.	225 mv as indicated on RF voltmeter.
11	Set the TUNE PWR switch to up at the test set.	At the transmitter, set the CARRIER ADJUST LOCAL switch to REMOTE.	Adjust potentiometer R14 (table 3–12) on automatic channel loading card A8 (fig. FO–48) as required.	200 mv as indicated on RF voltmeter.

Table 3–24. Frequency Synthesizer, Bench Performance Test

Step No.	Control settings: Test equipment	Control settings: Equipment under test	Test procedure	Performance standard
1	See para 3–32	See para 3–32	Connect a frequency counter to the RF translator (A1) assembly connector P5403.	

			Using the FREQUENCY SELECT thumbwheel switches on the test set, select each of the frequencies listed in table 3–5. After each setting, momentarily depress XMTR DTE pushbutton to tune the transmitter.	Frequencies observed at P5403 should be within tolerances specified in table 3–5. If frequencies are out of tolerance, refer to the bench troubleshooting chart step 5 for troubleshooting information.
2			Disconnect frequency counter from P5403 and connect it to P5404.	
			Using the FREQUENCY SELECT thumbwheel switches on the test set, select each of the frequencies listed in table 3–6. After each setting, momentarily depress XMTR DTE pushbutton to tune the transmitter.	Frequencies observed at P5404 should be within tolerances specified in table 3–6. If frequencies are out of tolerance, refer to the bench troubleshooting chart, step 5 for troubleshooting information.

CHAPTER 4

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

Section I. GENERAL MAINTENANCE INFORMATION

4-1. Introduction

This chapter provides the information necessary to maintain the transmitter at the general support maintenance level. These maintenance instructions are primarily intended to assist the repairman in determining whether the equipment is operating properly, and if not, to localize the malfunction to a fault at the plug-in card or module level. The scope of maintenance is assigned by the maintenance allocation chart (MAC). The maintenance information in this chapter includes, troubleshooting procedures, adjustments, removal and replacement, repair, performance test procedures, and performance standards such as voltage and resistance measurements. The order of presentation of this maintenance information is arranged in a sequence which is logical in terms of specific maintenance steps required to maintain the transmitter at the general support maintenance level.

4-2. Detecting Faulty Operation

Performance tests (paras 3-31 and 3-32) are provided for use in determining abnormal operation. Furthermore, indications of both normal and abnormal operation are given in the troubleshooting chart (para 4-24). Voltage and frequency measurements and waveforms are provided in section II of chapter 3 to further aid in fault detection.

4-3. Locating Trouble

The bench troubleshooting chart (para 4-24) is provided to aid in locating trouble in a minimum amount of time.

4-4. Checking Serviceability

General support testing procedures designed to check the serviceability of repaired items of equipment are included in section IV.

4-5. Correcting Trouble

The following information is included to aid in correcting equipment trouble that causes faulty operation:

a. Corrective measures are given in each troubleshooting chart.

b. Instructions for removing and replacing faulty equipment are given in paragraphs 3-29, 4-27, and 4-28.

c. Procedures for making the frequency synthesizer (A2) adjustments are given in paragraph 4-26. Partial disassembly of the frequency synthesizer (A2) is necessary in order to perform these adjustments; therefore, disassembly and reassembly instructions are given in paragraph 4-27.

4-6. Troubleshooting Techniques

The troubleshooting techniques in paragraph 3-6 are applicable to general support level troubleshooting.

4-7. Bench Testing

All adjustments, troubleshooting, and performance testing at general support level shall be performed with the transmitter removed from the equipment rack (unit 6) and placed on the workbench. Refer to paragraph 3-32 for bench test procedures.

4-8. Transmitter Interchangeability

Instructions for swapping transmitters within the equipment rack (unit 6) are given in paragraph 3-8.

4-9. Troubleshooting Data

Refer to paragraph 3-9 for troubleshooting data applicable to general support level troubleshooting.

4-10. Waveform Analysis

Refer to paragraph 3-10 for information concerning waveform analysis.

4-11. Voltage and Frequency Measurements

Refer to paragraph 3-11 for voltage and frequency measurement information.

4-12. Blown Fuses

Refer to paragraph 3-12 for information pertaining to blown fuses.

4-13. Reference Designation Number Locations

For information concerning the reference designation numbering system, refer to paragraph 3-13. Reference designation number locations of repairable parts are shown in the applicable parts location diagrams.

4-14. Replacing Parts

Parts replacement at general support level shall be in accordance with those procedures given in paragraph 3-14.

4-15. Isolating by Parts Substitution

Parts substitution at general support level shall be in accordance with those procedures given in paragraph 3-15.

4-16. Intermittents

For information pertaining to the troubleshooting of intermittently faulty components, refer to paragraph 3-16.

4-17. Cable Checks

Cable checks at general support level shall be performed in accordance with those procedures given in paragraph 3-17.

4-18. Tools and Test Equipment

Special tools (table 4-1) and test equipment (table 4-2) are required for general support maintenance as authorized by the maintenance allocation chart (MAC). Equivalent instruments may be used unless otherwise stated.

Table 4-1. Special Tools for General Support

Item No.	Description	Part No.	Qty
1	Printed circuit card extractor	985-050-001	1
2	31-Pin printed circuit card extender	233-00-029	1
3	41-Pin printed circuit card extender	233-00-038	1
4	RF translator extender cable	233-00-924	1
5	Synthesizer extender cable	233-00-913	1
6	RF extender cables	233-00-914	10
7	Synthesizer printed circuit card extender	233-00-036	1
8	Capacitor alignment tool	JFD5284	1
9	Inductor alignment tool	Cambion 2033-1	1

Table 4-2. General Support Maintenance Test Equipment

Nomenclature	Name	FSN
AN/USM-207	Digital readout electronic counter	6625-911-6368
ME-30A/U	Meter voltmeter	6625-643-1760
AN/URM-145	Electronic voltmeter	6625-973-3986
CN-796/U	Variable attenuator	5985-087-2547
R-390A/URR	Radio receiver	5820-538-7555
AN/URM-127	Signal generator	6625-783-5965
8491A HP	20-db Fixed attenuator	
T324732A	Receiver-Transmitter Test Set	
AN/USM-281	Oscilloscope	6625-053-3112
CN-16A/U	Transformer	5950-235-2886
ME-303/U	Multimeter	6625-902-7140
ME-202/U	Differential voltmeter	6625-709-0288

4-19. Parts Location Diagrams

The locations of transmitter assemblies replaced at general support level are illustrated in figure FO-51. Locations of the frequency synthesizer (A2) assembly subassemblies are illustrated in figure 4-7.

Section II. TROUBLESHOOTING AT GENERAL SUPPORT

4-20. General

This section provides troubleshooting data at the general support maintenance level for the T-1021/TSC-38B transmitter. Troubleshooting the transmitter consists of testing the unit at various levels to determine where the malfunction has occurred, and then either performing readjustment or replacement of the defective assembly or module. Paragraph 4-24 provides the troubleshooting information necessary for determining which part is malfunctioning. Perform troubleshooting in accordance with the procedures described in paragraph 4-6.

4-21. Reference Data

The reference data provided in paragraph 3-21 is also applicable to the troubleshooting procedures in this section.

4-22. Physical Test and Inspection

The physical test and inspection procedures in paragraph 3-22 are also applicable to general support level troubleshooting.

4-23. Use of Troubleshooting Charts

Refer to paragraph 3-23 for information concerning the use of the troubleshooting chart.

4-24. Troubleshooting Test Conditions

Refer to paragraph 3-24*b* for bench troubleshooting test conditions.

Chart 4-1. Bench Troubleshooting Chart

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
	Warning: Voltages capable of causing injury or death may be present on J4, K301, fuses, and power supply terminals.			
1	Refer to paragraph 3-24*b* for transmitter bench setup and power turn-on procedures.	*a.* POWER indicator (DS301) illuminates.	POWER indicator (DS301) fails to illuminate.	*a.* Remove fuse indicator F301 (upper) and remove fuse. Reinstall fuse indicator and observe that fuse indicator illuminates to indicate the presence of ac power. If ac power is present, reinstall fuse F301 and replace lamp DS301. If ac power is not present, reinstall fuse F301. Set the test set PWR switch to off and on and observe relay K301 actuating. *b.* If relay K301 actuates, place VOM ac probes on K301 pin 9 and chassis ground. 120V should be observed. (*a*) If 120 Vac is present higher category maintenance is required. (*b*) If 120 Vac is not present, replace relay K301. *c.* If relay K301 does not actuate place positive probe of VOM, on K301 pin 1 and negative probe on chassis ground. If +28 Vdc is present replace relay K301. If +28 Vdc is not present, higher category maintenance is required.
		b. Fuse indicator F301 (upper) not illuminated.	Fuse indicator F301 (upper) illuminated.	Replace blown fuse. Fuse indicator should not illuminate. *a.* If fuse indicator does not illuminate, proceed to step 2. *b.* If fuse indicator illuminates, higher category maintenance is required.
		c. Fuse indicator F302 (lower) not illuminated.	Fuse indicator F302 (lower) illuminated.	Replace blown fuse. Fuse indicator should not illuminate. *a.* If fuse indicator does not illuminate proceed to step 2.

				b. If fuse indicator illuminates disconnect P3801 from synthesizer A2, P5405 from RF translator (A1), and remove transmit gain control PC card A4. Replace blown fuse; fuse indicator should not illuminate. If fuse indicator does not illuminate, reconnect each assembly one at a time until fuse indicator illuminates; then replace failed assembly and fuse. If fuse indicator illuminates higher category maintenance is required.
	DC Voltage Checks: **Caution:** Insure receiver power is off before removing or replacing modules.			
2	*a.* Reinstall transmit gain control control A4 PC card using 31-pin extender card A20 (para 3–29*b*).			
	b. Using a differential voltmeter, measure dc voltage at J307 pin A.	+20 ±0.1 Vdc	*a.* Voltage out of tolerance. *b.* No output voltage.	Adjust +20 Vdc power supply A11 output voltage (para 3–28*b*). Replace +20 Vdc power supply A11 (para 4–28*a*).
3	Using a differential voltmeter, measure dc voltage at J307 pin *k*.	−20 ±0.1 Vdc	*a.* Voltage out of tolerance. *b.* No output voltage.	Adjust −20 Vdc power supply circuit on the signal control PC card A5 (para 3–28*c*). *a.* Replace signal control PC card A5 (para 3–29*b*) and remeasure output voltage. If −20 Vdc is present, proceed to step 4. If −20 Vdc is not present, check for −28 Vdc on J306 pin C. *b.* If −28 Vdc is present, remove the transmit gain control A4 PC card, automatic channel loading A8 PC card, and synthesizer A2 cable P3801. Systematically reinstall each cable and assembly until defective module is isolated. Replace defective module. *c.* If −28 Vdc is not present, replace −28 Vdc power supply A19 (para 4–28*c*).
4	Using a differential voltmeter, measure dc voltage at J307 pin B.	+6.4 ±0.05 Vdc	*a.* Voltage out of tolerance.	Adjust +6.4 Vdc power supply A10 output voltage (para 3–28*a*).

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
			b. No output voltage.	Replace +6.4 Vdc power supply A10 (para 4–28*b*).
	System Tuning Check:			
5	At the test set (T324732A) select 29.9990 MHz on the FREQUENCY SELECT thumbwheel switches and depress the XMTR DTE push-button.	XMTR DTE indicator lamp on test set illuminates for less than 5 seconds.	XMTR DTE indicator lamp remains illuminated and transmitter does not tune.	*a.* Connect a test cable with a 1X probe between the vertical INPUT of a test oscilloscope and test point TP8 on transmit gain control card A4 (fig. FO–51). Set oscilloscope as follows: TRIGGERING --- MAIN INT SWEEP MODE -- NORM MAGNIFIER ---- X1 TIME/DIV ------ 10MS/CM VOLTS/DIV ----- 2 *b.* Depress the XMTR DTE pushbutton on the test set while observing the oscilloscope. A momentary 40-ms pulse at +4 ±0.5V amplitude should be observed. *c.* If a 40-ms pulse is not present, measure the input to the TGC card A4 between J307 pin P and ground with a multimeter set to dc volts. Depress the XMTR DTE pushbutton on the test set. 0 Vdc level should be observed. If the 0 Vdc level is not obtained, higher category maintenance is required. *d.* If the 0 Vdc level is correct, and the 40-ms pulse is not present, replace transmit gain control card A4 (para 3–29*b*). *e.* If the 40-ms pulse is correct and the 0 Vdc level is present, and replacement of A4 does not correct the failure, continue to steps 6 and 7.
	RF Carrier Checks:			
6	Connect the test set +0.75V jack to the TGC VOLTAGE test jack on the transmitter front panel. Connect the 50-ohm terminated probe of the RF voltmeter to the 20-db at-	A 0.45 Vrms or greater level should be present on the RF voltmeter.	Voltage out of tolerance.	*a.* At the test set, set the KEY switch to the down position and connect the 20-db attenuator (fig. 3–2) to J5401 on the RF translator using a BNC/TNC

tenuator (fig. 3–2). At the test set, set KEY switch to up position and PC switch to the up position.

Sealectro Adapter. Set KEY switch to the up position; 0.45 Vrms or greater level should be indicated. If voltage is correct, reconnect coaxial cable P5401 to J5401.

b. If the 0.45 V or greater level is not correct, connect the 50-ohm RF voltmeter probe to P5402 (RF input) at RF translator (A1). A 100-kHz signal of 25 to 60 mv amplitude should be present. Connect a test cable between RF translator (A1) P5403 (pump) and the digital electronic counter plug-in unit INPUT jack. Set counter controls as follows:

INPUT ---------- PLUG-IN
TIME BASE ----- 1 SEC
FUNCTION ----- FREQ
FREQ DIAL ----- 60

A frequency readout of 1000.000 kHz ±3 Hz which corresponds to 61 MHz should be observed; record this indication. Move the test cable from P5403 at RF translator A1 to P5404. Set counter FREQ DIAL to 90. A 899.0000 kHz ±3 Hz readout corresponding to 90.899 MHz should be indicated; record this indication. If the signals of P5403, and/or P5404 are incorrect proceed to step 7. If signals at P5402 P5403 and P5404 are correct and the 0.45 Vrms signal is incorrect, replace RF translator module A1 (para 3–29*c*). If replacement of RF translator (A1) does not correct the fault, measure voltage levels at P5405 of RF translator A1 (refer to table 3–7). If any voltages measured are incorrect, higher category maintenance is required.

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				c. If at P5402 the 100-kHz signal measured is not correct, insert signal control card A5 into the transmitter chassis on a 31-pin extender card (para 3–29*b*). Connect oscilloscope 1X probe to J306 pin j on the signal control PC card A5. Set oscilloscope controls as follows: TIME BASE .. 10 μsec/cm VERT ..... 50 mv/cm MAIN SWEEP .. NORMAL TRIGGERING ... INTERNAL ac. A signal level of 30 mv to 100 mv p-p at 100 kHz should be observed. (1) If the signal at J306 pin j is present, replace or repair the coaxial cable between J306 pin j and RF translator A1 P5402. (2) If the signal at J306 pin j, is not present, set transmitter POWER ON/OFF switch (S1) to OFF and place ohmmeter test leads to J306 pin b (EXCITER KEY) and ground. A ground indication less than 10 ohms should be indicated. (3) Place ohmmeter test leads between J306 pin c (CARRIER ENABLE) and ground. A ground indication less than 10 ohms should be indicated. (4) Set transmitter POWER ON/OFF switch (S1) to ON. Connect oscilloscope 1X probe to J306 pin e. Set oscilloscope controls as follows: TIME BASE ... 10 μsec/cm VERT ..... 100 mv/cm MAIN SWEEP . NORMAL TRIGGERING . INTERNAL ac.

				A 100-kHz signal of 350 ±250 mv p-p should be observed. If this signal is not present, replace synthesizer A2 (para 3–29*d*). If the problem still exists, higher category maintenance is required.
				d. If all the indications of the preceding step are correct, replace signal control card A5 (para 3–29*b*).
				e. If replacing the signal control card A5 does not correct the problem, higher category maintenance is required.
	Transmitter Frequency Checks.			
7	Connect a test cable between the counter SIGNAL INPUT AC jack and the 20-db attenuator at transmitter output jack J1 (fig. 3–2). At receiver-transmitter test set select the band edge frequencies (from 2.0000 to 29.9999 MHz listed in table 3–5 on FREQUENCY SELECT thumbwheel switches. Depress XMTR DTE pushbutton after each frequency is selected.	The frequency indicated on the counter should be the digits selected on the FREQUENCY SELECT thumbwheel switches ±3 Hz.	Frequency out of tolerance.	*a.* If the frequency observed is not correct, connect a test cable from counter high frequency plug-in unit to pump input connector P5403 on RF translator (A1). Perform frequency functional test procedure as follows: (1) Preset the thumbwheel switches on the test set to the frequencies shown in table 3–5, (Digit Checks). The pump frequency 10 MHz through 1 kHz digits should follow the sequence given. If any individual digits are not correct, refer to the note in table 3–6 for corrective action. (2) If step (1) does not correct the pump frequency fault, proceed to 1–6-MHz VCO checks shown in table 3–5. If the pump frequency becomes unstable, perform synthesizer 5-MHz clock adjustment (para 3–28*d*), and synthesizer alignment procedure (para 4–26). After alignment, perform frequency checks in tables 3–5 and 3–6.

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				(3) If synthesizer alignment does not correct the frequency instability and step 1 does not correct the fault, replace frequency synthesizer A2 (para 3–29*d*).
				(4) Connect counter plug-in test cable to 1st L.O. input at P5404 of the RF translator A1 assembly. The frequency should correspond to those listed in table 3–5 for each selected 100-Hz frequency change of the thumbwheel switch.
				(5) If the 100-Hz digits are not correct, refer to corrective action note in table 3–6.
				b. If the above step does not correct the 100-Hz digit fault, replace frequency synthesizer (A2) (para 3–29*d*). If problem still exists after replacement of the frequency synthesizer (A2), higher category maintenance is required.
				c. Connect a test cable from counter frequency input to synthesizer jack J3804 (fig. 4–7②). A 100 kHz ±0.1 Hz signal should be observed. If signal amplitude is too low for a stable counter presentation, connect jack J3804 to an ac voltmeter input jack (HP 400D or equivalent). Connect the counter frequency input to the voltmeter output jack. The voltmeter range switch may be changed until the counter indication is observed. If the 100-kHz signal is incorrect, replace frequency synthesizer A2 (para 3–29*d*).

8	*Tune Power Check:* At the test set, set TUNE PWR switch to on (up position) and KEY switch to on (up position). Set RCVR XMTR NORMAL LEVELS switch to XMTR PWR. Select any frequency between 2 and 29.9999 MHz on the FREQUENCY SELECT thumbwheel switches. Depress XMTR DTE pushbutton.	The NORMAL LEVELS meter should indicate +6 db.	The NORMAL LEVELS meter indicates RF power output too low.	*a.* Connect the RF voltmeter with 50-ohm termination to the 20-db attenuator as shown in figure 3–2. The RF voltmeter level should be 0.4 ±0.05 Vrms. If the level is below that required, connect the 50-ohm RF voltmeter probe to P5402 of the RF translator (A1) using a Sealectro to BNC/TNC adapter. The level should be 30 ±10 mVrms at 100 kHz. *b.* If the signal level at P5402 is correct, replace rf translator (A1) (para 3–29*c*.) If the signal level at P5402 is not correct, place signal control card A5 on a 31-pin extender card (para 3–29*b*). Place oscilloscope X1 probe to J306 pin e of A5. Set oscilloscope controls as follows: VERT ..... 100 mv/cm HORIZ ..... 10 μsec/cm MAIN SWEEP .. NORMAL TRIGGERING ... INTERNAL AC. A 100-kHz signal with amplitude of 255 ±105 mv p-p should be observed. *c.* If the 100-kHz signal amplitude is correct, perform signal control card A5 ALC adjustment procedure (para 3–28*h*). If readjustment fails to correct problem, replace signal control card A5 (para 3–29*b*). *d.* If replacement of A5 does not correct the malfunction, measure signal control card A5 voltage inputs as shown in table 3–7. If any input signals are not correct, higher category maintenance is required.

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
	TGC Function Check:			
9	Set the test set PC switch to ON (up position), KEY switch to ON (up position), and TUNE PWR switch to ON (up position). Verify that the TGC switch (S1) located on the transmit gain control A4 PC card (table 3–12) is in the ON position. Connect a dc voltmeter (negative) to the TGC terminal on test set and adjust TGC potentiometer for a −7 Vdc level. *Note:* The +0.75 Vdc level normally connected to the TGC VOLTAGE test point on trasmitter front panel should be removed during this test. Connect the 50-ohm RF voltmeter probe to the 20-db attenuator at transmitter jack J1 (fig. 3–2).	The RF voltmeter should indicate 0.4 ±0.05 Vrms.		
10	Set TUNE PWR switch to off (down position) at the test set.	The RF voltmeter should indicate a level below 100 mVrms, and should not be scanning.	*a.* RF voltmeter is scanning.	Vary the TGC potentiometer above and below the −7 Vdc level indicated on the dc voltmeter until scanning stops. If the scanning stops and the dc voltmeter level is not −7 ±0.6V, perform the TGC card alignment procedure (para 3–28*e*). If alignment does not correct the problem, replace TGC card A4 (para 3–29*b*).
			b. RF voltmeter does not scan, but indicates a level above 100 mVrms.	Place transmit gain control card A4 on the 31-pin extender card (para 3–29*b*). Connect positive lead of a dc voltmeter to J307 pin Z. A dc level of +5 ±1V should be observed. If the level is correct and TGC will not scan, perform the following steps: *a.* Place dc voltmeter to J307 pin X. A sweeping signal from +0.2V to +3.7 ±0.5 Vdc should occur. If the level is a steady dc level, replace TGC A4 card (para 3–29*b*).

	b. If the dc signal is sweeping and the RF signal is not scanning, higher category maintenance is required.
c. RF voltmeter scans up past 400 mVrms and reset to 0, and then continues scanning.	*a.* If scanning does not stop, perform TGC alignment procedure (para 3–28*e*).
	b. If TGC alignment does not correct the malfunction, connect the negative lead of a DCVM to J307 pin *h* and the positive lead to ground. The level should be −7 ±0.6V as set by the TGC potentiometer. Remove the test connection from pin *h* and connect it to J307 pin *d*. The level should be between −1.3 and −2.1 V. If this level is not corrrect, higher category maintenance is required.
d. RF voltmeter stops scanning at a level other than 400 mVrms.	*a.* If the TGC stops at an incorrect RF output level, adjustment of R5 (table 3–12) on the TGC card may be required. If more than two turns of R5 are required either cw or ccw, perform TGC alignment procedure (para 3–28*e*).
	b. If R5 or TGC alignment fails to correct TGC level, higher category maintenance is required.
e. TGC will not complete cycle (continues scanning) when the EXCITER GAIN on transmitter front panel is changed.	*a.* If EXCITER GAIN control on front panel is changed and TGC will not stop scanning, the rf gain is too low. Set EXCITER GAIN control fully cw. Apply a +0.75 Vdc signal to TGC VOLTAGE test point on transmitter front panel. Adjust R69 (table 3–12) on signal control card A5 for a 0.57 Vrms level as observed on the RF voltmeter. Remove the +0.75 Vdc from the TGC VOLTAGE test point.

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				b. Depress the XMTR DTE pushbutton on the test set. The TGC should stop when the −7V TGC sample level is applied. *c.* If steps *a* and *b* do not correct the fault, higher category maintenance is required.
11	*Modulation Checks:* All the test set and transmitter switch settings of para 3–24*b* should be as stated except for the following: *Note.* Using the test set +0.75V jack, apply +0.75V to the TGC VOLTAGE test jack on the transmitter front panel. *a.* Set AUDIO INPUT CH A2, CH A1, CH B1, CH B2 on the test set to ON and set KEY switch to up. *b.* Connect a test cable with a 1X probe between the vertical INPUT of a test oscilloscope and J306 pin j of signal control card A5 (fig. FO–51①). Set oscilloscope as follows: TRIGGERING ------ MAIN INT SWEEP MODE ---- NORM MAGNIFIER ------- X1 TIME/DIV --------- 0.1 *c.* Set OSC LVL at the test set fully cw. *d.* Set OSC select switch on the test set to each channel position (A1, B1, A2 and B2).	Oscilloscope should display a signal for each channel selection as shown in waveform i (fig. 3–4).	Signal amplitude low or loss of modulation signal at channel selected.	*a.* Connect oscilloscope 1X probe to J306 pin U of signal control card A5. See waveform g for signal control modulation input indication (fig. 3–4). *b.* If signal on J306 pin U is correct, perform signal control card A5 alignment (para 3–28*g* and *h*). *c.* If the alignment in step *b* above fails to correct problem, replace signal control card A5 (para 3–29*b*). *d.* If replacement of signal control card A5 does not correct fault,

connect oscilloscope 1X probe to J306 pin W. See waveform h for ACL input indication (fig. 3–4).

e. If the signal at pin W of J306 is not correct, replace automatic channel loading card A8 (para 3–29*b*).

f. If replacement of ACL card A8 does not correct the malfunction, higher category maintenance is required.

g. Select the input test point corresponding to the faulty channel as listed below, and connect oscilloscope to appropriate channel filter pair PC card A3 or A6 input pin:

	Channel	*Conn*	*Pin*
CH A1/B1 filter pair A3	A1	J302	W
	B1	J302	P
CH A2/B2 filter pair A6	A2	J304	W
	B2	J304	P

Set the oscilloscope as follows:

TRIGGERING ... MAIN INT
SWEEP MODE .. NORM
MAGNIFIER X1
TIME/DIV 0.2ms/cm
VOLTS/DIV 0.2V/cm

h. Set OSC select switch on the test set to the faulty channel and look for typical waveform (see fig. 3–4 waveform c).

i. If a good signal is present at the filter pair input pin, check the output of the channel being measured as listed below.

	Channel	*Conn*	*Pin*
CH A1/B1 filter pair A3	A1	J302	j
	B1	J302	A
CH A2/B2 filter pair A6	A2	J304	j
	B2	J304	A

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				j. If the signal is not present at the output of the channel filter pair being measured, replace the channel pair (A3 or A6) (para 3–29*b*).
				k. If the signal is not present at filter pair input pin, remove the test connection from the channel being measured. Select the input test point on the dual-balanced modulator corresponding to the faulty channel as listed below, and connect oscilloscope to appropriate input pin.

	Channel	*Conn*	*Pin*
Dual-bal mod A7	A1	J301	T
	B1	J301	V
Dual-bal mod A21	A2	J303	T
	B2	J303	V

See waveform (a) for typical waveform (fig. 3–4). If the signal is not present at pin T or V of A7 or A21, higher category maintenance is required (cable or connector problem).

(1) If the signal is present at pin T or V of A7, remove the test connection from pin T or V and connect it to pin L and then to pin b of A7. Set the oscilloscope as follows:

TRIGGERING -- MAIN INT
SWEEP MODE - NORM
MAGNIFIER -- X1
TIME/DIV ---- 10 ms/cm
VOLTS/DIV --- 0.1V/cm

The oscilloscope should display 100 kHz at each pin measured. If the 100 kHz is present at pin L and pin b, measure the output of

A7 at pins R (A1) and X (B1). If a signal is not present at pin R and/or pin X of A7, replace dual-balanced modulator A7 (para 3–29*b*). If a signal is present at pin R and/or pin X of A7, higher category maintenance is required. If the 100-kHz signal is not present at pin L and/or b, higher category maintenance is required.

(2) If the signal is present at pin T or V of A21, remove the test connection from pin T or V. Select the input test point on dual-balanced modulator A21 corresponding to the faulty channel listed below, and connect the oscilloscope to the appropriate multiplex carrier generator input signal.

Channel	*Connector*	*Pin*
A2	J303	L
B2	J303	b

Set the oscilloscope as follows:

TRIGGERING	INT
SWEEP MODE	NORM
MAGNIFIER	X1
TIME/DIV	5 μsec/cm
VOLTS/DIV	0.2

The oscilloscope should display 106.29 kHz at pin L (see waveform (d)), or 93.71 kHz at pin b (see waveform (e), fig. 3–4).

(*a*) If the waveforms are present at pins L and b of A21, measure the output of A21 at pins X (B2) and/or R (A2). If signal is not present at pin X and/or R of A21, replace channel A2, B2 dual-balanced modulator A21 (para 3–29*b*).

Step No.	Procedure	Normal indication	Abnormal indication	Corrective measures
				If a signal is present at pins X and R of A21, a higher category maintenance is required. (*b*) If the waveforms are not present at pins L and/or b of dual-balanced modulator A21, measure the output of multiplex carrier generator A9 at pin *d* or F of A9. If a waveform is not present, replace multiplex carrier generator A9 (para 3–29*b*). (*c*) If the waveform is present at pin *d* or F of A9, higher category maintenance is required.

Section III. MAINTENANCE OF TRANSMITTER

4-25. General

This section consists of step-by-step instructions for adjustment, removal and replacement, disassembly and reassembly, and repair procedures which are required to maintain the transmitter and its subassemblies at the general support maintenance level as authorized by the maintenance allocation chart (MAC).

4-26. Frequency Synthesizer Adjustment (fig. FO-50).

NOTES

1. During the following adjustment procedures, some voltage ranges may not be possible to obtain because of circuit changes due to aging. The select-in-test (SIT) components as identified on applicable schematics were chosen initially to provide these voltage ranges. Replacement of these components is a higher category function.

2. If a screwdriver adjustment is sealed with cementing compound, apply Glyptal thinner GC-67 before making adjustment.

3. Use capacitor alignment tool JFD-5284 to adjust miniature capacitors. Use inductor alignment tool CAMBION 2033-1 to adjust inductors and trimmer resistors.

All switch settings referred to in the following adjustment procedures are located on the test set front panel unless otherwise specified. All pushbuttons are momentarily depressed unless otherwise specified. For information concerning the test set, refer to Operation and Maintenance Manual, Receiver-Transmitter Test Set (Raytheon part No. T324732A).

a. Synthesizer Bench Setup Procedure.

(1) Remove transmitter from equipment rack unit 6 (para 3-29*a*) and place on workbench.

(2) Remove frequency synthesizer (A2) assembly from the transmitter chassis (para 3-29*d*).

(3) Remove frequency synthesizer A2 assembly cover (para 4-27).

(4) Using the extender cables supplied with the test set, connect the synthesizer A2 assembly to the transmitter chassis (fig. 4-1).

(5) Connect the transmitter to the test set in accordance with procedures in paragraph 3-24*b*.

(6) Allow 1/2-hour warmup period before performing frequency synthesizer adjustments.

b. 1-6-MHz Control Loop Adjustments (figs. 4-2 and 4-3).

(1) Disconnect P2 (fig. FO-50) from the hf VCO (A2A3) assembly and connect to frequency counter FREQ A jack (fig. 4-2). Set counter SENSITIVITY control to 1V.

(2) Remove cover plates from RF box No. 2 A2A6 (para 4-27) and connect oscilloscope probe to A2A6J2 pin 4 (FO-50). Set oscilloscope controls to 2V/cm, 2 msec/cm and dc int positive trigger.

(3) Adjust R31 (fig. FO-50) on the 1-6-MHz phase-lock loop card A2A6A2 ccw to produce a waveform on the oscilloscope as shown in figure 4-3(a). The RCVR DTE indicator illuminates.

(4) Note upper and lower amplitude levels of waveform (a) and readjust R31 cw for a dc level midway between upper and lower levels observed. The RCVR DTE indicator should extinguish.

(5) Set oscilloscope sweep control to 0.5 sec/cm. Set the FREQUENCY SELECT switches to 02.0000 and depress RCVR DTE pushbutton. Counter should indicate 1.001 MHz ±3 Hz.

(6) Set the FREQUENCY SELECT switches to 06.9990 and depress RCVR DTE pushbutton. Observe that the length of time for the signal to lock, as indicated by the transient interval from the start of the pulsating waveform to the midway dc level (fig. 4-3(b)), is 3 seconds or less. Counter should indicate 6.0 MHz ±3 Hz. Adjust R31 as required to maintain sweep time under 3 seconds.

(7) Set the FREQUENCY SELECT switches to 02.0000 and depress RCVR DTE pushbutton. Observe that the length of time for the signal to lock, as indicated by the transient interval from the start of the pulsating waveform to the midway dc level (fig. 4-3(b)), is 3 seconds or less.

(8) Connect a differential voltmeter to A2-A6J2-pin 14 (fig. 4-2).

(9) Change the FREQUENCY SELECT switches to each setting listed below and depress

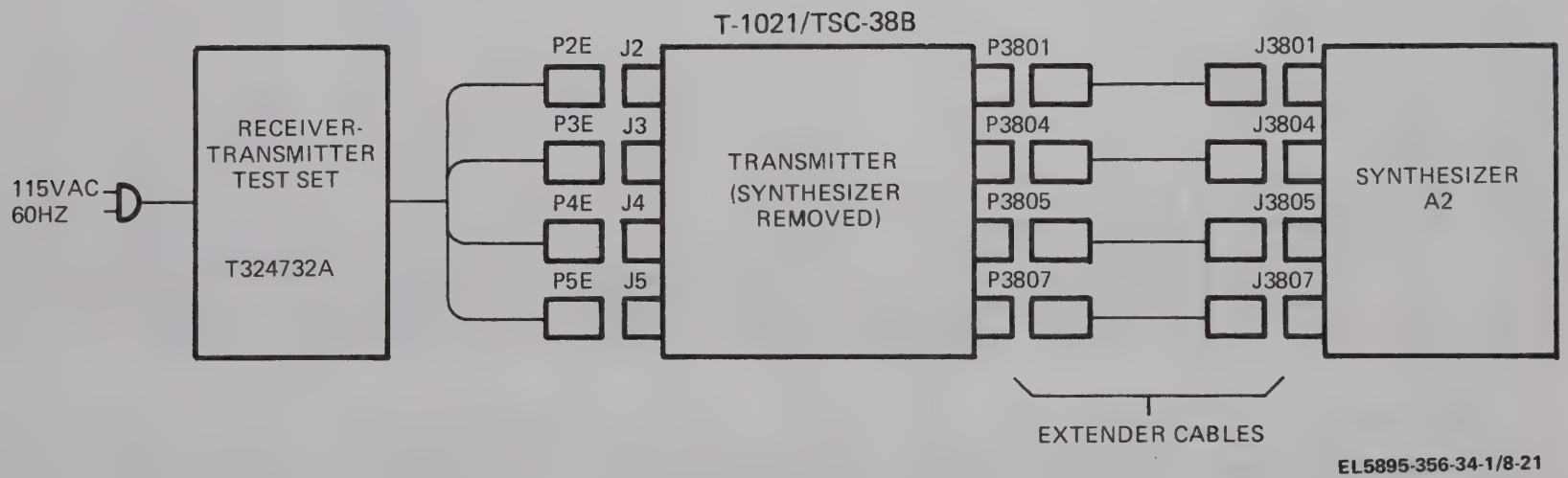


Figure 4–1. Synthesizer/test set, connection diagram.

RCVR DTE pushbutton each time. Verify that the dc voltage on the voltmeter is more positive than −2.5 Vdc and that the counter reads the correct frequency.

Frequency select switches	*Counter frequency*
020000	1001±.003 kHz
022000	1201±.003 kHz
025000	1501±.003 kHz
029000	1901±.003 kHz
034000	2401±.003 kHz
040000	3001±.003 kHz
048000	3801±.003 kHz
058000	4801±.003 kHz

(10) Change the FREQUENCY SELECT switches to each setting listed below and depress RCVR DTE pushbutton after each new setting. Verify that the dc voltage on the differential voltmeter is less than +15 Vdc and the counter reads the correct frequency.

Frequency select switches	*Counter frequency*
021990	1200.000±.003 kHz
024990	1500.000±.003 kHz
028990	1900.000±.003 kHz
033990	2400.000±.003 kHz
039990	3000.000±.003 kHz
047990	3800.000±.003 kHz
057990	4800.000±.003 kHz
069990	6000.000±.003 kHz

(11) Disconnect the differential voltmeter and oscilloscope probes from the synthesizer.

(12) Change the FREQUENCY SELECT switches to each setting listed below and depress RCVR DTE pushbutton after each new setting. Verify that the counter reads the correct frequency.

Frequency select switches	*Counter frequency*
066880	5689.000±.003 kHz
066770	5678.000±.003 kHz
066660	5667.000±.003 kHz
066550	5656.000±.003 kHz
066440	5645.000±.003 kHz
066330	5634.000±.003 kHz
066220	5623.000±.003 kHz
066110	5612.000±.003 kHz

(13) Disconnect the counter from A2A3P2 and reconnect A2A3P2 to A2A3J2 on the hf VCO assembly.

(14) Reinstall RF box No. 2 cover (para 4–27).

c. Hf VCO Adjustment (fig. 4–4).

(1) Remove hf VCO cover (para 4–27).

(2) Connect the frequency counter to the synthesizer (A2) pump output jack J3806 (fig. FO–50). Set counter controls as follows:

DIRECT/HETERODYNE	DIRECT
FUNCTION	FREQ
GATE TIME	1 SEC
SENSITIVITY	PLUG-IN
INPUT switches	0.3V MAX

(3) Set the FREQUENCY SELECT switches to 2.0000 and depress RCVR DTE. The counter should indicate 88.999 MHz ±3 Hz.

(4) Connect oscilloscope probe to TP2 (fig. FO–50) on hf VCO (A2A3) assembly. The oscilloscope should display a steady dc voltage of +11 ±1 Vdc. If required, adjust A2A3A2R57 (or A2A3A2R50) (fig. FO–50).

(5) On the hf VCO (A2A3) assembly, connect the differential voltmeter proble to C3. The differential voltmeter should indicate +7 ±0.05-V. If necessary adjust C9 (fig. FO–50).

(6) Connect differential voltmeter probe to A2A3TP1 (fig. FO–50).

(7) Set the FREQUENCY SELECT switches to 06.9990 and depress RCVR DTE pushbutton. Counter should read 84.000 MHz ±3 Hz. Voltmeter should read +3.5 ±0.5 Vdc. If required, adjust A2A3A1R7 (fig. FO–50) for the proper dc voltage at A2A3TP1 (fig. FO–50).

(8) Set the FREQUENCY SELECT switches to 02.0000 and depress RCVR DTE pushbutton. Counter should read 88.999 ±3 Hz. Voltmeter should read +14.5 ±1.0 Vdc. If required, adjust A2A3A1R9 (fig. FO–50) for the proper dc voltage at A2A3TP1.

(9) Repeat steps (7) and (8) above until no further adjustment of R7 or R9 is required.

(10) Change FREQUENCY SELECT switches from 02.0000 to 06.9990 and observe change in dc voltage on oscilloscope A2A3TP2 after RCVR DTE pushbutton is depressed and the RCVR DTE lamp is extinguished. Voltage change should not exceed 1.0 Vdc. Adjust C17 (or C25) on the control loop board A2A3A2 (fig. FO–50) to minimize dc change and repeat this step.

NOTE

This adjustment is very sensitive and should be performed with great care. It may be necessary to adjust A2A3A2R57 (or A2A3A2R50) (fig. FO–50) in conjunction with A2A3A2C17 (or A2A3-A2C25) to achieve the +11 ±1 Vdc balance over the 1-to-6-MHz VCO range.

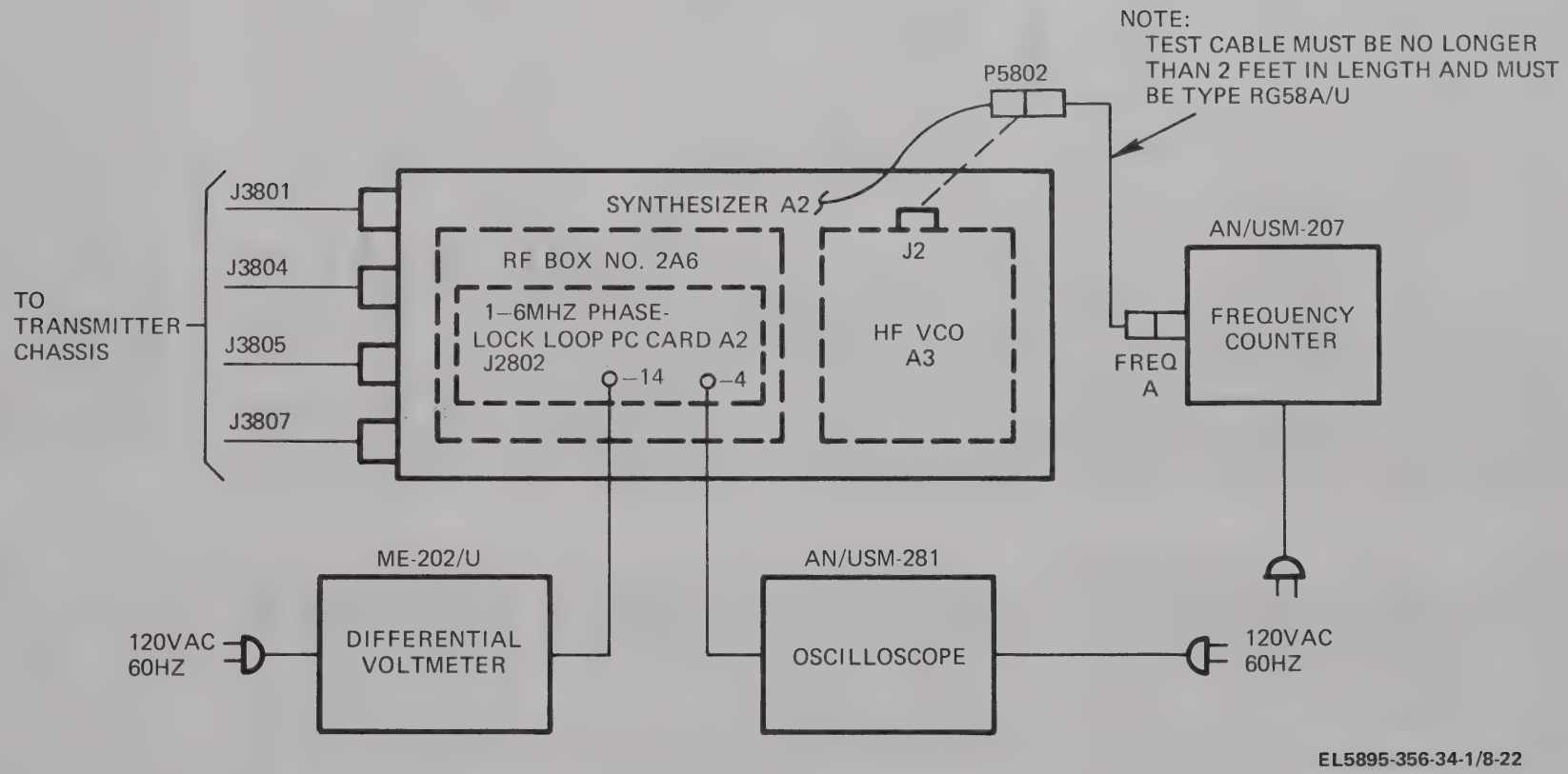
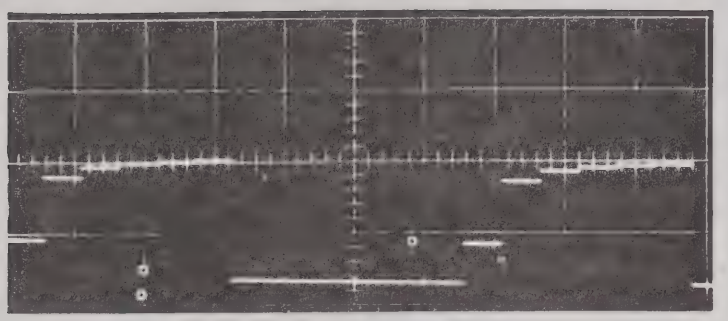


Figure 4–2. 1–6-MHz control loop adjustment, test equipment setup.

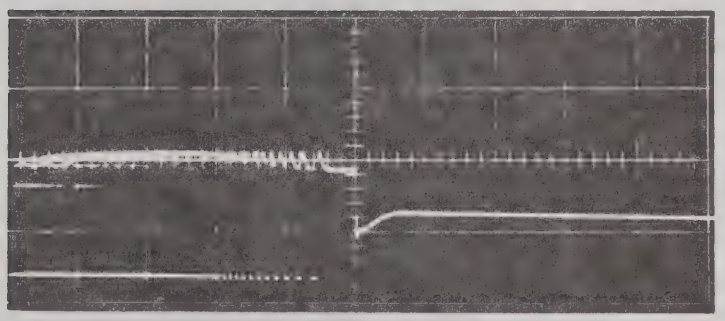
(A)



TEST POINT: J2802-4
OSCILLOSCOPE SETTINGS: 5V/CM, 2 MSEC/CM
DC INT POS TRIGGER

1-6 MHZ VCO FINE CONTROL VOLTAGE (UNLOCKED CONDITION).

(B)



TEST POINT: J2802-4
OSCILLOSCOPE SETTINGS: 5V/CM, 0.5 SEC/CM
DC INT POS TRIGGER

1-6 MHZ VCO LOOP LOCKING TIME DURATION FOR A
02.0000 MHZ TO 06.9990 MHZ TRANSITION.

NOTE:
WAVEFORMS ARE VIEWED USING A TEKTRONIX
545A OSCILLOSCOPE WITH TYPE 53/54B PLUG-IN.

EL5895—356—34—1/8—23

Figure 4-3. 1-6-MHz control loop, waveforms.

(11) Set FREQUENCY SELECT switches to 11.9990 and depress RCVR DTE pushbutton. Counter should read 79.000 MHz ±3 Hz. Voltmeter should read +3.5 ±0.5 Vdc. Adjust A2A3A1R17 for +3.5 ±0.5 Vdc at A2A3TP1.

(12) Set FREQUENCY SELECT switches to 07.0000 and depress RCVR DTE pushbutton. Counter should read 83.9990 MHz ±3 Hz. Voltmeter should read ±14.5 ±1.0 Vdc. Adjust A2A3A1R19 for +14.5 ±1.0 Vdc at A2A3TP1.

(13) Repeat steps (11) and 12) above until no further adjustments of R17 and R19 are required.

(14) Repeat steps (11) and (12) above for VCO bands 3 through 6. Frequencies and voltages should read as shown below.

VCO band	*Frequency select switches*	*Counter frequency*	*Voltage nominal*	*Adjust Pot A2A3A1*
3 (80 MHz)	169990	74.000	+3.5±0.5	R27
	120000	78.999	+14.5±1.0	R29
4 (75 MHz)	219990	69.000	+3.5±0.5	R37
	170000	73.999	+14.5±1.0	R39
5 (70 MHz)	269990	64.000	+3.5±0.5	R47
	220000	68.999	+14.5±1.0	R49
6 (65 MHz)	299990	61.000	+7±1.0	R57
	270000	63.999	+14.5±1.0	R59

(15) Disconnect counter, oscilloscope, and differential voltmeter from synthesizer.

(16) Reinstall hf VCO cover (para 4–27).

d. RF Section 2nd L.O. Adjustments.

(1) *9.1-MHz control loop adjustment.*

(*a*) Remove covers from the RF section L.O. (A2A4) assembly (para 4–27).

(*b*) Connect oscilloscope probe to A2A5-C8 (fig. FO–50) on front of RF box No. 1. Set the 100-Hz FREQUENCY SELECT switch to the 9 position and depress RCVR DTE pushbutton. Oscilloscope should display an ac ramp of less than 100 millivolts p-p at an average dc level of 2.0 to 2.6 volts.

(*c*) Adjust A2A4 L2 (fig. FO–50) of RF section second L.O. until the dc level of signal is at 2.2 Vdc.

(*d*) Set 100-Hz FREQUENCY SELECT switch to the 0 position and depress RCVR DTE pushbutton. Observe that the control loop voltage on the oscilloscope has changed to a dc level between 3.4 and 4.2 Vdc.

(2) *90.899-MHz oscillator adjustment.*

(*a*) Connect oscilloscope probe to lead of R57 (E12) (fig. FO–50) on differential amplifier board in RF section, second L.O. (A2A4) assembly.

(*b*) Connect the frequency counter to the frequency synthesizer (A2) assembly second L.O. output connector (J3807 or J3808).

(*c*) Set 100 Hz FREQUENCY SELECT switch to 5 position and depress RCVR DTE pushbutton. Oscilloscope should show a dc level between 8 and 12 volts with no observable ac component. The frequency counter should indicate a frequency of 90.8995 MHz. If either of these two conditions are not indicated, the 90.899 MHz oscillator is not phase-locked.

(*d*) Adjust A2A4C114 (fig. FO–50) for an increase in dc level at E12 until an ac signal appears on oscilloscope and frequency counter reading becomes unstable. Note dc level where instability (loss of phase-lock) occurs (approximately +17 V).

(*e*) Adjust C114 for a decrease in dc level at E12 until an ac signal appears on oscilloscope and frequency counter reading becomes unstable. Note dc level where instability (loss of phase-lock) occurs (approximately +4V to +6V).

(*f*) Adjust C114 for a dc level midway between the upper and lower levels noted in steps (*d*) and (*e*) above.

(*g*) Set 100-Hz FREQUENCY SELECT switch to 0 position and depress RCVR DTE pushbutton. Frequency counter should read 90.8990 MHz ±3 Hz.

(*h*) Momentarily interrupt power to the test set; then reconnect power. The 90.8999 MHz oscillator should lockup again at 90.8990 MHz.

(*i*) Change 100-Hz FREQUENCY SELECT switch from 0 to 9, one position at a time, depressing the RCVR DTE pushbutton each time. Each frequency as indicated on the frequency counter changes from 90.8990 MHz to 90.8999 MHz, in 100-Hz steps. The 100-Hz figure should correspond to the figure on the 100-Hz FREQUENCY SELECT switch within a tolerance of ±3 Hz.

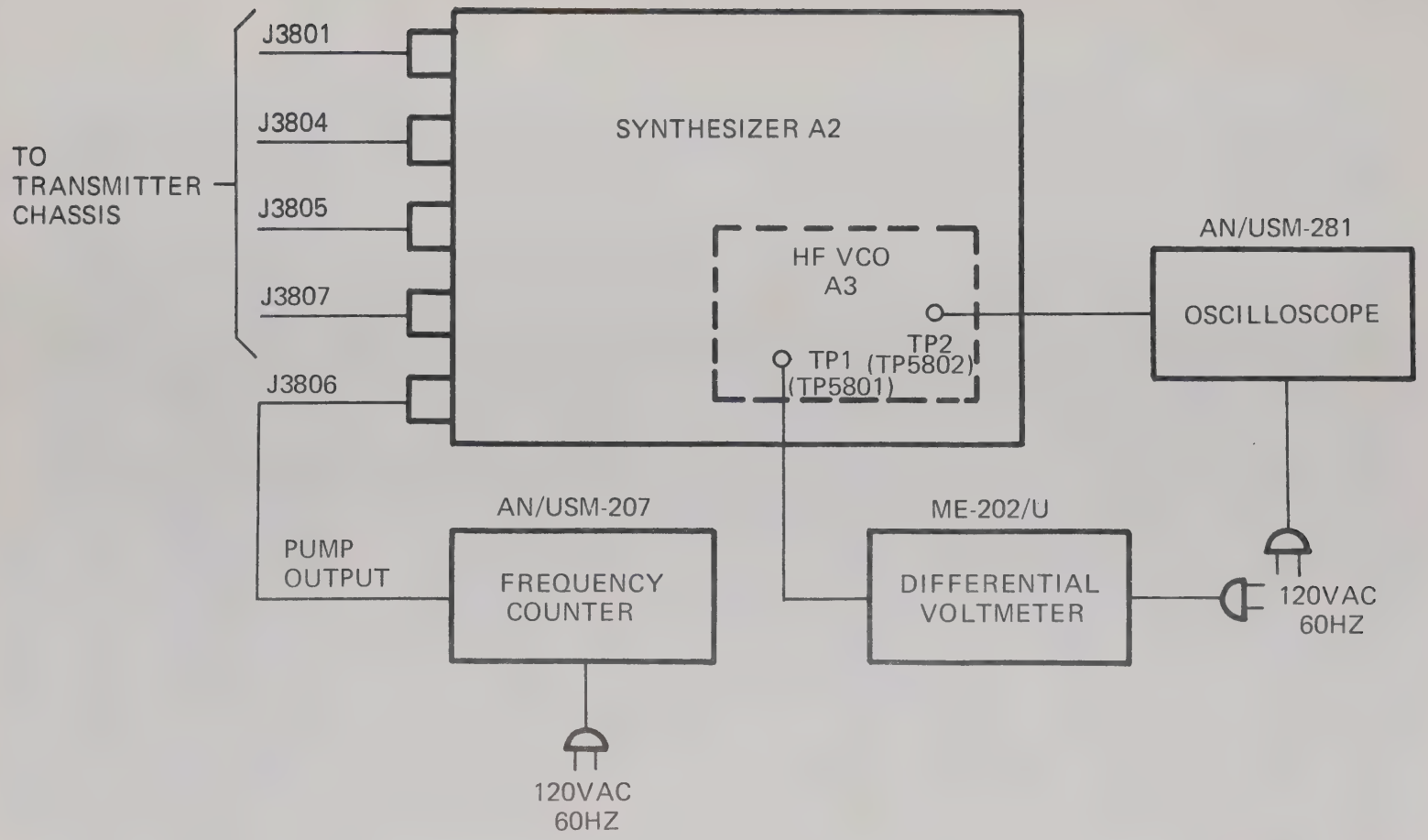


Figure 4–4. Hf VCO adjustment test equipment setup.

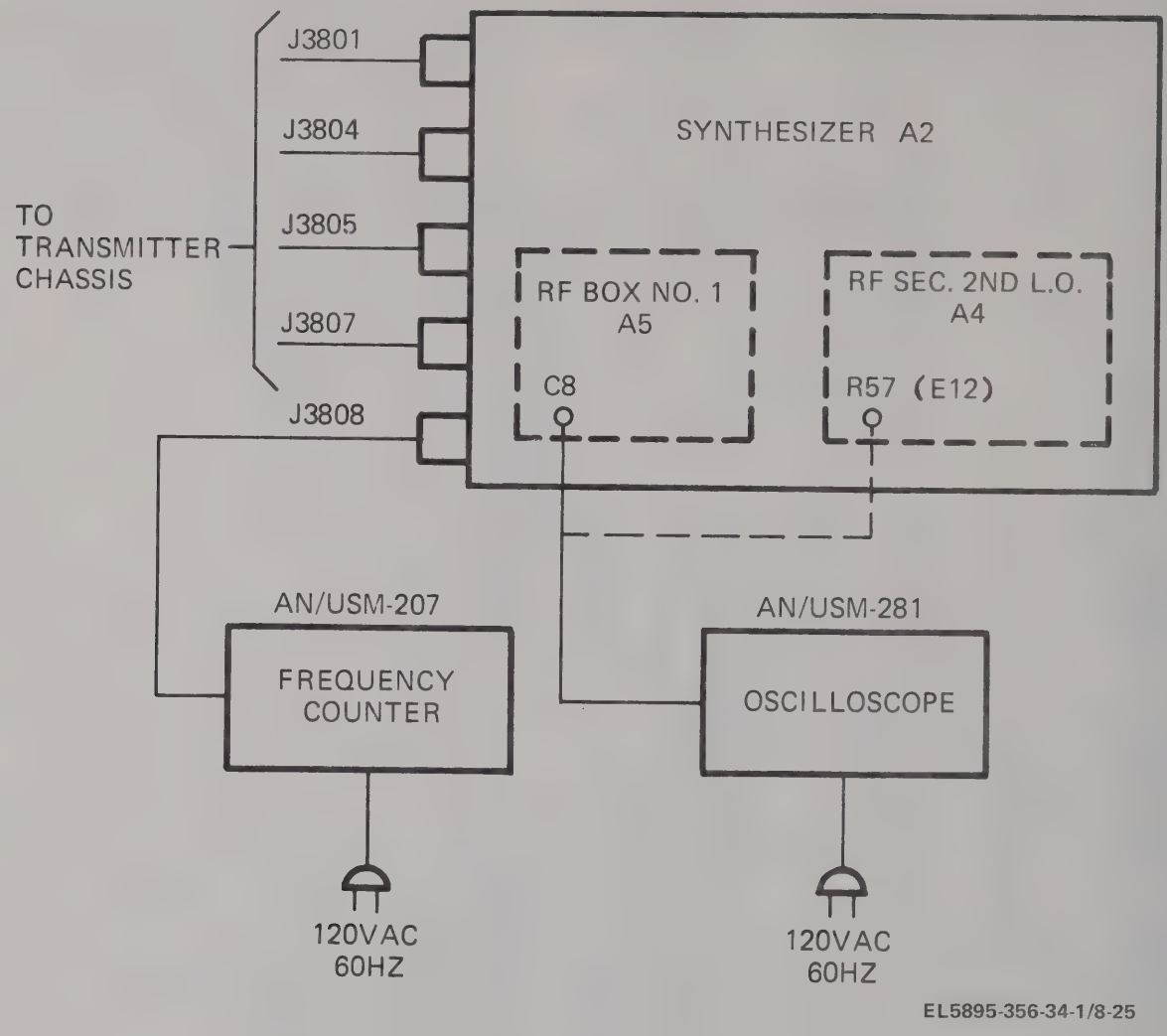


Figure 4–5. RF section 2nd L.O. adjustments, test equipment setup.

(*j*) With the 100-Hz FREQUENCY SELECT switch set to 9, interrupt power to the test set; then reconnect power. The 90.899 MHz oscillator should lockup again at 90.8999 MHz.

(*k*) Disconnect oscilloscope and frequency counter, and reinstall cover on RF section second L.O. (A2A4) assembly (para 4–27).

4–27. Frequency Synthesizer A2 Disassembly and Reassembly Procedure

a. Disassembly. Remove the frequency synthesizer cover (fig. 4–6) by removing eight bottom screws and five end screws. Frequency Synthesizer subassembly locations are shown in figure 4–7. To gain access to the test points and adjustments perform the appropriate disassembly procedures below.

(1) *RF section, 2nd L.O.* Remove four screws and remove the cover. Removal of the entire RF section, 2nd L.O. assembly, is a higher category maintenance function.

(2) *RF box No. 1.* To remove PC cards, remove four screws (one in each corner of the end plate) and remove the plate. Remove PC cards in accordance with procedures in paragraph 3–29*b*. Gaining access to the filter section is a higher category maintenance function.

(3) *RF box No. 2.* To remove PC cards, remove the four screws (one in each corner of the end plate) and remove the plate. Remove PC cards in accordance with procedures in paragraph 3–29*b*. Gaining access to the filter section is a higher category maintenance function.

(4) *Hf VCO.* To gain access to the test points and adjustments in the 2nd L.O. remove six screws and remove the cover. Removal of the entire hf VCO assembly is a higher category maintenance function.

b. Reassembly. Reassembly procedures for synthesizer subassemblies are the reverse of those for disassembly.

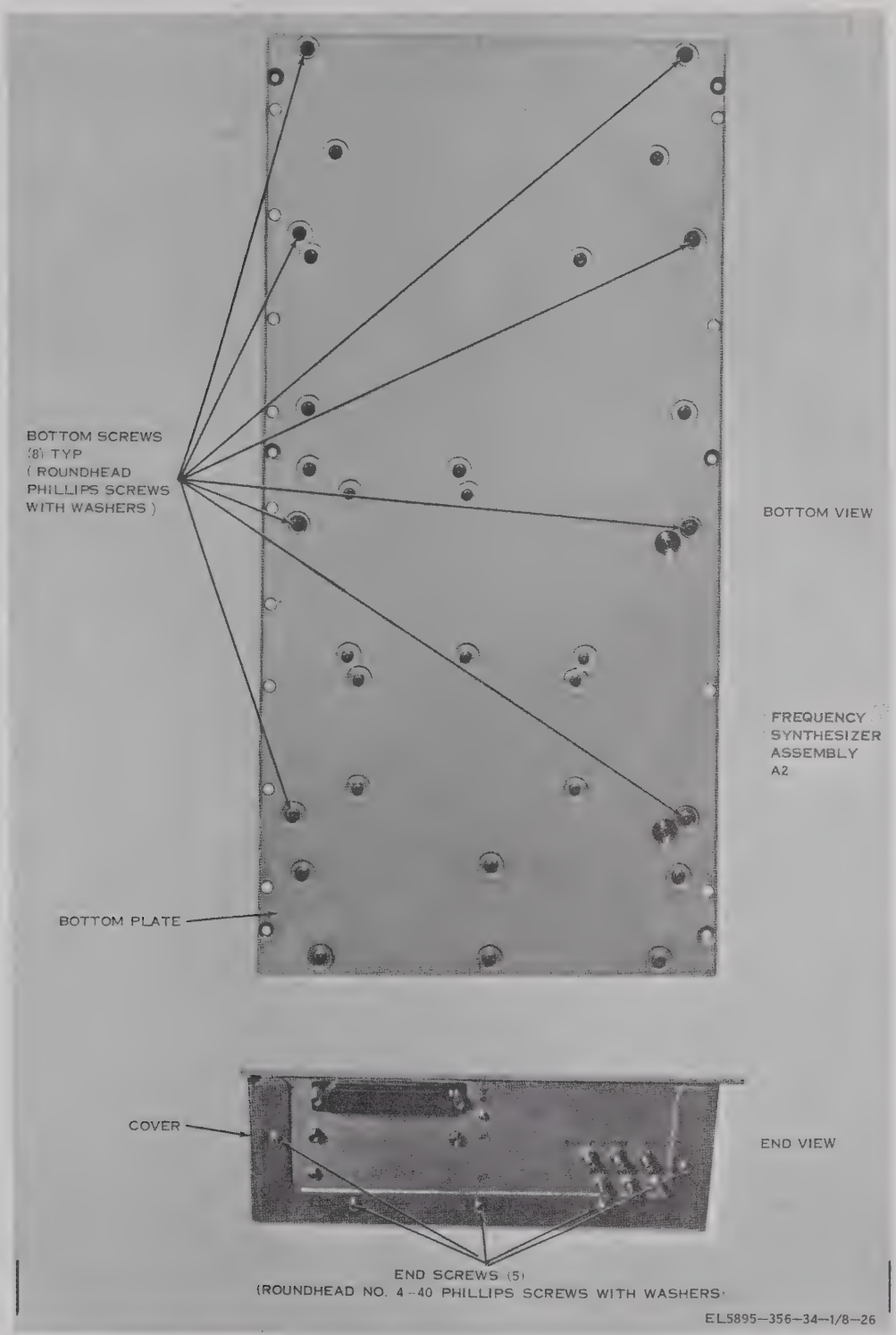


Figure 4-6. Frequency synthesizer (A2), cover removal.

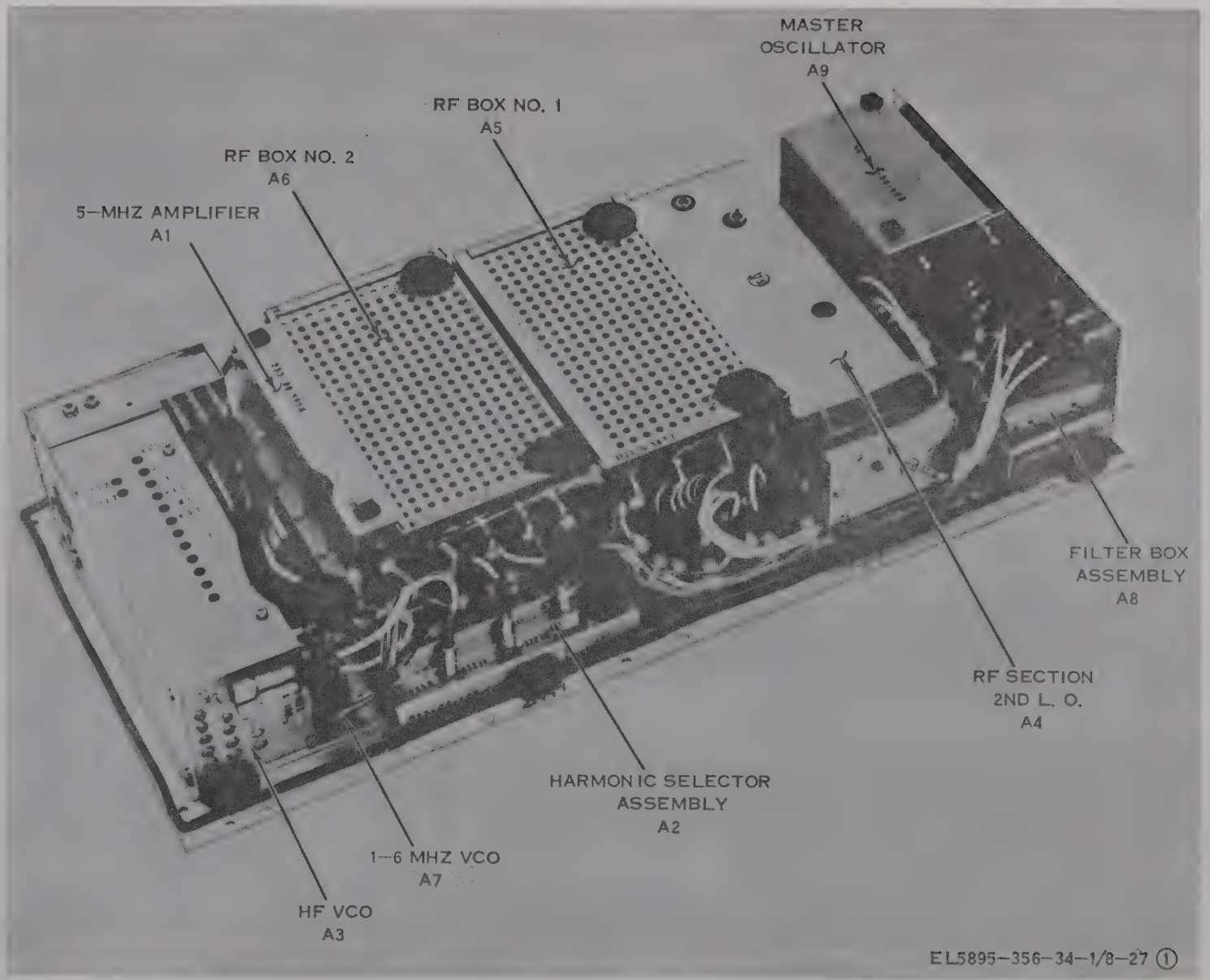


Figure 4-7①. Frequency synthesizer (A2), parts location diagram (sheet 1 of 3).

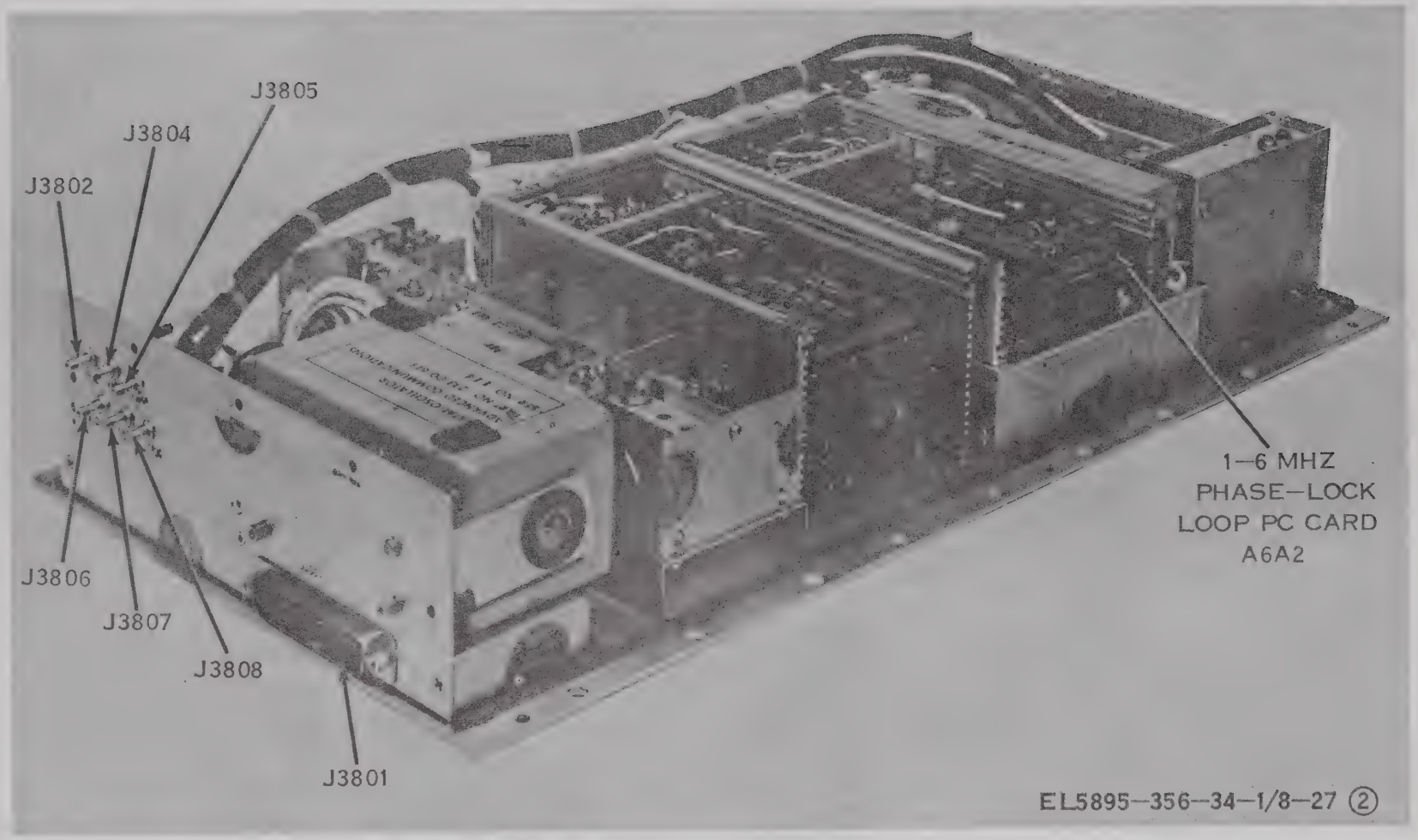


Figure 4–7②. Frequency synthesizer (A2), parts location diagram (sheet 2 of 3).

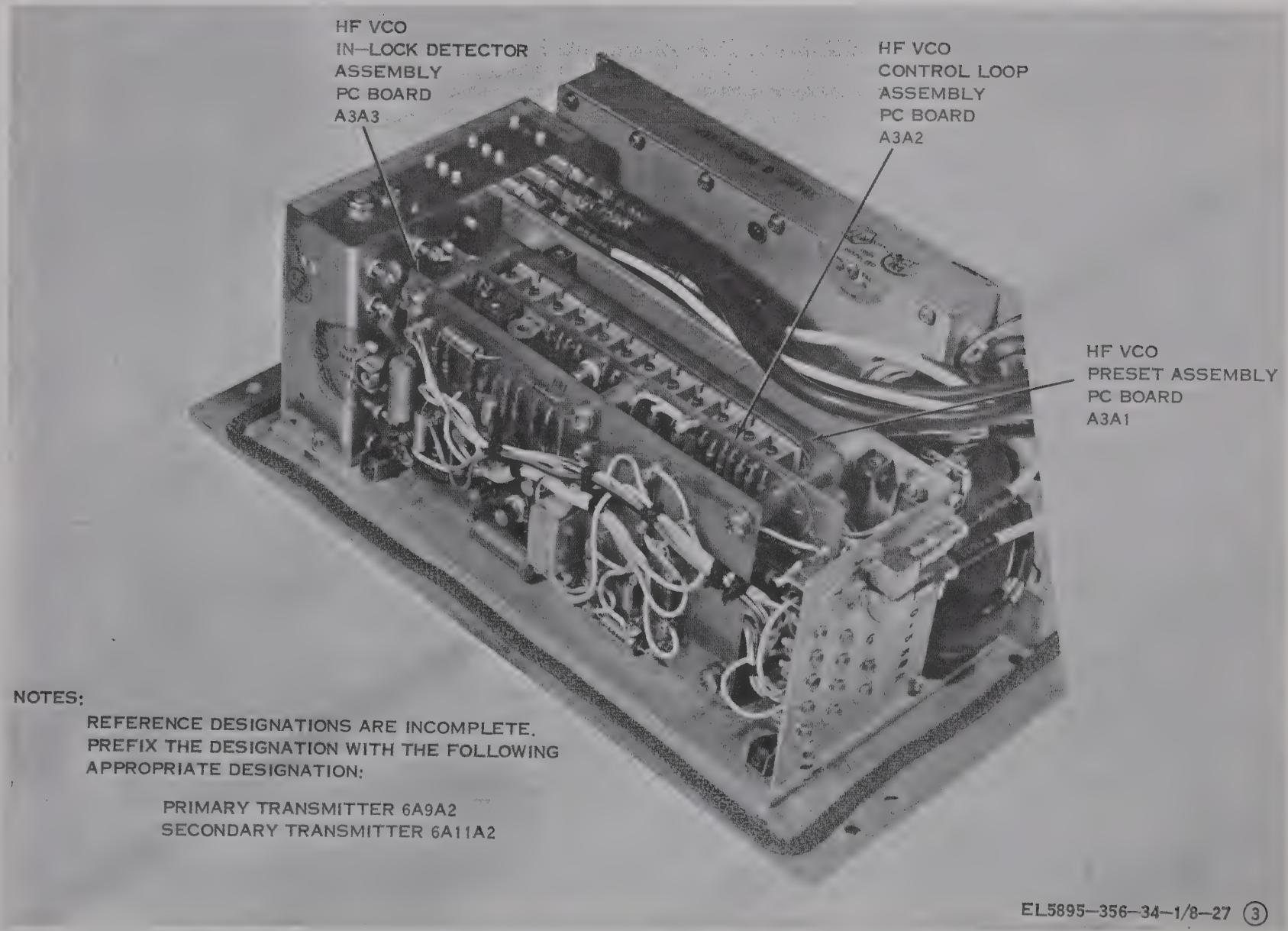


Figure 4-7③. Frequency synthesizer (A2), parts location diagram (sheet 3 of 3).

4-28. Removal and Replacement Procedures

a. +20 Vdc Power Supply A11.

(1) *Removal.*

(*a*) Remove transmitter top cover (para 3-29*a*).

(*b*) Remove six mounting screws and transmitter front panel (fig. 4-8).

NOTE

The TGC VOLTAGE test point must be disconnected with a soldering iron.

(*c*) Remove two screws securing bracket used for retaining PC card extraction tool (fig. FO-51①).

(*d*) Remove the RF translator assembly A1 (para 3-29*c*).

(*e*) Remove the three screws securing the power supply to the left side of the transmitter chassis; then remove the four screws securing the power supply to the chassis front panel of the transmitter (fig. 4-8).

(*f*) Turn the power supply to allow access to screws on the terminal strip.

WARNING

Voltages capable of causing injury or death may be present on the terminal strip.

(*g*) Tage and disconnect the leads connected to the terminal strip on the power supply.

(*h*) Lift the power supply free from the chassis.

NOTE

If the power supply is to be replaced with one of similar form and fit, the standoff mounting bracket that secures the unit to the left side of the drawer must be attached to the replacement unit.

(2) *Replacement.* Replacement procedures for the +20 Vdc power supply are the reverse of those for removal.

b. +6.4 Vdc Power Supply A10.

(1) *Removal.*

(*a*) Remove the transmitter from the rack and place on work bench (para 3-29*a*).

(*b*) Remove the +20 Vdc power supply A11 from the transmitter chassis (para 4-28*a*).

(*c*) Remove the frequency synthesizer A2 from the transmitter chassis (para 3-29*d*).

(*d*) Remove two screws securing resistor (R319) bracket and remove bracket (fig. FO-51③).

(*e*) Remove and lay to one side the POWER ON/OFF switch (S301). Place keeper, lockwasher, and nut back onto switch to prevent loss.

(*f*) Tag and disconnect leads from the terminal strip on the power supply.

(*g*) Remove the remaining two screws securing the power supply to the chassis center divider.

(*h*) Remove the remaining four screws securing the sliding rail and spacer to the right side of the drawer and remove sliding rail and spacer.

(*i*) Remove printed circuit card from connector J314 (fig. FO-48).

(*j*) Remove the card divider plate (shield) separating the card basket and power supply by removing eight screws; three securing the shield to the drawer side, three on the center divider, and two on the bottom plate of the card basket.

(*k*) While supporting the power supply, remove three screws on the front side of the drawer. Be ready to catch three spacers as power supply is lifted free from transmitter chassis.

NOTE

When the three front panel screws are removed, the three spacers that position the power supply with respect to the front side of the drawer are unsecured. Since the spacing is critical, make certain that the spacers are returned to their original position when the power supply is replaced.

(2) *Replacement.* Replacement procedures for the +6.4 Vdc power supply are the reverse of those for removal.

c. -28 Vdc Power Supply A19.

(1) *Removal.*

(*a*) Remove the transmitter from the rack (para 3-29*a*), turn the transmitter over and reinstall the transmitter in an upsidedown position.

(*b*) Disconnect P4 from back of transmitter (fig. FO-51④).

(*c*) Remove transmitter bottom cover plate.

(*d*) Remove frequency synthesizer assembly A2 (para 3-29*d*).

(*e*) Tag and disconnect the leads from the terminal strip on the -28 Vdc power supply.

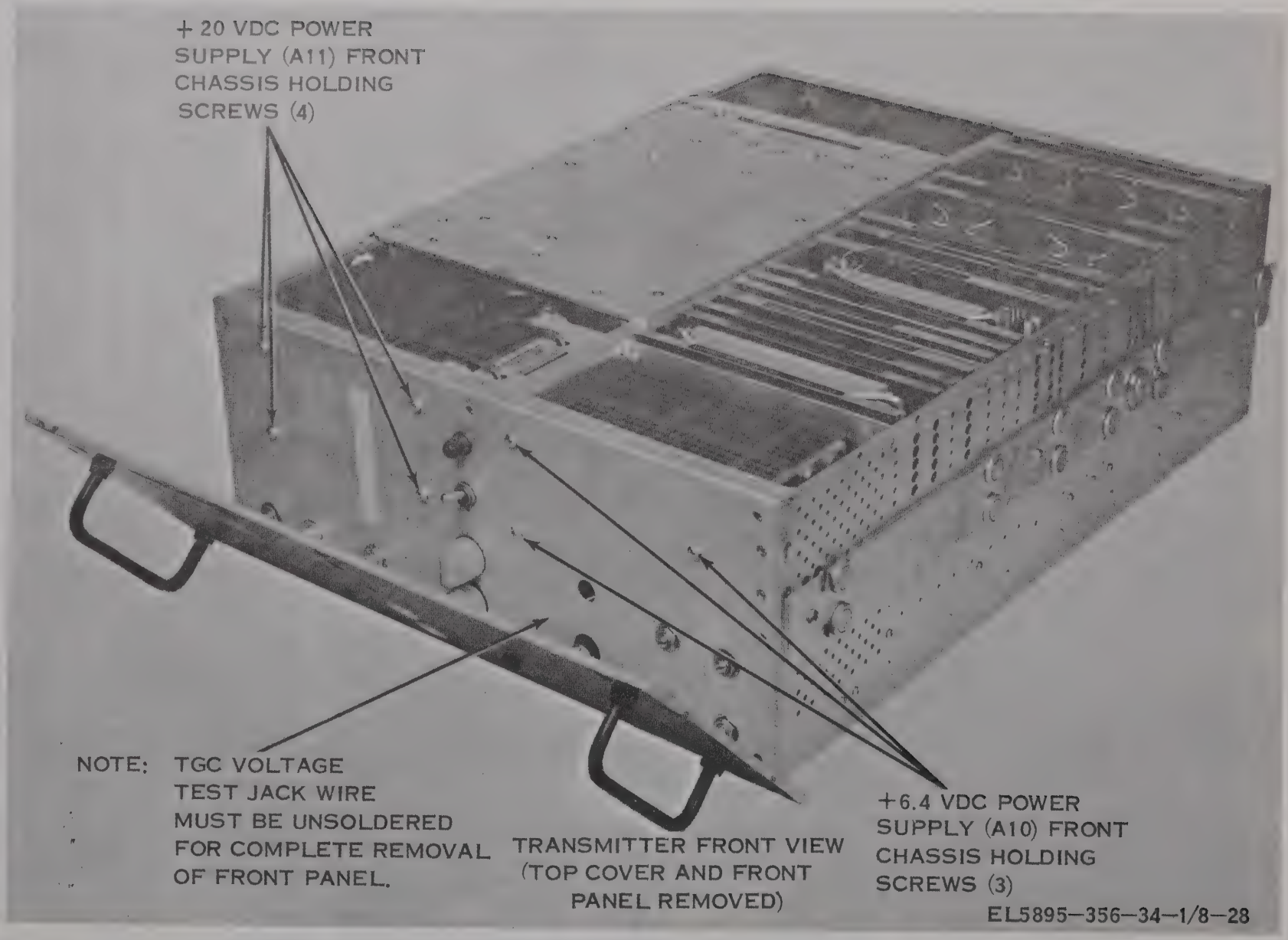


Figure 4-8. Transmitter power supply removal.

(*f*) While supporting the power supply, remove the four screws securing it to the center divider; then lift the unit free from the transmitter chassis.

(2) *Replacement.* Replacement procedures for the −28 Vdc power supply are the reverse of those for removal.

Section IV. GENERAL SUPPORT TESTING

4–29. General

Transmitters repaired at general support level shall be tested in accordance with the performance tests in section IV of chapter 3.

INDEX

	Paragraph	Page
Adjustment and alignment procedures (*See* Direct maintenance).		
ALC sample (*See* Functional description).		
Amplifier A2A1 5-MHz (fig. FO-28) (*See* Circuit analysis).		
Automatic channel loading A8 PC card (*See* Circuit analysis).		
Automatic channel loading card A8 adjustment (*See* Direct maintenance).		
Band control A16 (*See* Circuit analysis).		
Bench testing (*See* General maintenance information).		
Bench transmitter performance test (*See* Direct support testing).		
Bench troubleshooting (*See* Troubleshooting at direct support).		
Bench troubleshooting chart (*See* Maintenance information).		
Blown fuses (*See* General maintenance information *and* Maintenance information).		
Buffer amplifier A2A2A2 (fig. FO-31) (*See* Circuit analysis).		
Cable checks (*See* General maintenance information *and* Maintenance information).		
Carrier adjust (*See* Functional description).		
Carrier enable (*See* Functional description).		
Carrier, 100-kHz (*See* Functional description).		
Channel enable (*See* Functional description).		
Channel filter pairs A3/A6 (*See* Circuit analysis).		
Checking serviceability (*See* General maintenance information *and* Maintenance information).		
Circuit analysis:		
Control analysis	2-11	2-15
Automatic channel loading A8 PC card	2-11*d*	2-22
Front panel controls	2-11*a*	2-15
Signal control A5 PC card	2-11*b*	2-18
Transmit gain control A4 PC card	2-11*c*	2-20
Frequency select analysis	2-13	2-27
Band control A16	2-13*b*	2-27
Code conversion matrices A17 and A18	2-13*c*	2-30
Frequency select memory A13, A14, and A15	2-13*a*	2-25
Frequency synthesizer A2 analysis	2-14	2-31
Filter box A2A8 (fig. FO-43)	2-14*e*	2-48
Hf (pump) signal generating section	2-14*b*	2-32
Harmonic generator (fig. FO-29)	2-14*b*(3)	2-39
Buffer amplifier A2A2A2 (fig. FO-31)	2-14*b*(3)(*b*)	2-40
Harmonic selector A2A2 (fig. FO-30)	2-14*b*(3)(*a*)	2-40
Logic control A2A2A1 (fig. FO-33)	2-14*b*(3)(*d*)	2-40
Video amplifier and mixer A2A2A3 (fig. FO-32)	2-14*b*(3)(*c*)	2-40
Hf (pump) VCO loop	2-14*b*(1)	2-35
Hf (pump) VCO A2A3 (fig. FO-24)	2-14*b*(1)(*a*)	2-35
Hf (pump) VCO control loop A2A3A2 (fig. FO-25)	2-14*b*(1)(*b*)	2-35
Control loop A2A3A2 (fig. FO-25①)	2-14*b*(1)(*b*)*1*	2-35
Control loop A2A3A2 (fig. FO-25②)	2-14*b*(1)(*b*)*2*	2-37
Hf (pump) VCO preset A2A3A1 (fig. FO-26)	2-14*b*(1)(*c*)	2-38
In-lock indicator A2A3A3 (fig. FO-27)	2-14*b*(1)(*d*)	2-38
1-6-MHz VCO loop	2-14*b*(4)	2-40
Variable divider-synthesizer pump A2A6A1 (fig. FO-35)	2-14*b*(4)(*b*)	2-42
1-6-MHz phase-lock loop A2A6A2 (fig. FO-36)	2-14*b*(4)(c)	2-45
1-6-MHz VCO A2A7 (fig. FO-34)	2-14*b*(4)(*a*)	2-42
5-MHz amplifier A2A1 (fig. FO-28)	2-14*b*(2)	2-39
L.O. signal generating section	2-14*c*	2-45
Second L.O. RF section A2A4 (figs. FO-37 and FO-38)	2-14*c*(1)	2-45
Second L.O. variable divider A2A5A2 (figs. FO-39 and FO-40)	2-14*c*(2)	2-47
Master clock signal generating section	2-14*a*	2-31

	Paragraph	Page
RF box No. 1 A2A5 and RF box No. 2 A2A6 (figs. FO–41 and FO–42)	2–14*d*	2–48
General	2–9	2–13
Modulator analysis	2–10	2–13
Channel filter pairs A3/A6	2–10*b*	2–13
Dual-balanced modulator A7/A21	2–10*a*	2–13
Multiplex carrier generator A9	2–10*c*	2–14
Power supply analysis (fig. FO–5)	2–15	2–48
Power supply PS–1 (−28 VDc) A19 (fig. 2–12)	2–15*a*	2–49
Power supply PS–2 (+20 Vdc) A11 (fig. FO–44)	2–15*b*	2–49
Power supply PS–3 (+6.4 Vdc) A10 (fig. FO–45)	2–15*c*	2–49
RF translator A1 analysis	2–12	2–23
Converter assembly A1A2	2–12*a*	2–23
Filter box A1A4	2–12*f*	2–25
Low-pass filter A1A5	2–12*b*	2–24
Preamplifier A1A1	2–12*c*	2–24
Video amplifier A1A3	2–12*d*	2–25
−7 Vdc amplifier regulator A1A6	2–12*e*	2–25
Code conversion matrices A17 and A18 (*See* Circuit analysis).		
Control (*See* Functional description).		
Control analysis (*See* Circuit analysis).		
Control loop adjustments, 1–6 MHz (*See* General maintenance).		
Control loop A2A3A2 (fig. FO–25① and ②) (*See* Circuit analysis).		
Control loop, 9.1 MHz (*See* General maintenance).		
Converter assembly A1A2 (*See* Circuit analysis).		
Correcting trouble (*See* General maintenance information *and* Maintenance information).		
Description (*See* Description and data).		
Description and data:		
Description	1–4	1–2
Tabulated data	1–5	1–2
Detecting faulty operation (*See* General maintenance information *and* Maintenance information).		
Direct maintenance:		
Adjustment and alignment procedures	3–28	3–49
Automatic channel loading card A8 adjustment	3–28*f*	3–53
Frequency synthesizer A2 5-MHz clock adjustment	3–28*d*	3–51
Signal control card A5 ALC and TGC alignment	3–28*h*	3–53
Signal control card A5 AM level adjustment	3–28*g*	3–53
Signal control card A5 −20 Vdc adjustment	3–28*c*	3–51
Transmit gain control (TGC) card A4 alignment	3–28*e*	3–52
+6.4 Vdc power supply A10 adjustment	3–28*a*	3–49
+20 Vdc power supply A11 adjustment	3–28*b*	3–51
General	3–27	3–49
Removal and replacement procedures	3–29	3–55
Frequency synthesizer assembly A2	3–29*d*	3–57
Removal	3–29*d*(1)	3–57
Replacement	3–29*d*(2)	3–58
Printed circuit (PC) cards	3–29*b*	3–55
Removal	3–29*b*(1)	3–55
Replacement	3–29*b*(2)	3–55
RF translator assembly A1	3–29*c*	3–56
Removal	3–29*c*(1)	3–56
Replacement	3–29*c*(2)	3–57
Transmitter chassis (6A9 or 6A11)	3–29*a*	3–55
Disassembly	3–29*a*(2)	3–55
Reassembly	3–29*a*(3)	3–55
Removal	3–29*a*(1)	3–55
Replacement	3–29*a*(4)	3–55
Direct support testing:		
Bench transmitter performance test	3–32	3–69
Documents	3–32*c*	3–69
General	3–32*a*	3–69
Initial test equipment settings	3–32*e*	3–69
Test connections and conditions	3–32*d*	3–69

	Paragraph	Page
Test equipment and materials	3-32*b*	3-69
General	3-30	3-58
Rack-mounted transmitter performance test	3-31	3-58
General	3-31*a*	3-58
Initial test equipment settings	3-31*d*	3-59
Test connections and conditions	3-31*c*	3-58
Test equipment and materials	3-31*b*	3-58

Documents (*See* Direct support testing).
Dual balanced modulator A7/A21 (*See* Circuit analysis).

Filter box A1A4 (*See* Circuit analysis).
Filter box A2A8 (fig. FO-43) (*See* Circuit analysis).
Frequency select analysis (*See* Circuit analysis).
Frequency select memory A13, A14, and A15 (*See* Circuit analysis).
Frequency select section (*See* Functional description).
Frequency synthesizer A2 (*See* Functional description).
Frequency synthesizer A2 analysis (*See* Circuit analysis).
Frequency synthesizer adjustments (*See* General maintenance).
Frequency synthesizer disassembly and reassembly procedure (*See* General maintenance).
Frequency synthesizer 5-MHz clock adjustment (*See* Direct maintenance).
Front panel controls (*See* Circuit analysis).
Functional description:

Control (fig. FO-3)	2-4	2-4
Frequency select section (fig. 2-3)	2-6	2-8
Hf (pump) VCO band (preset) signals	2-6*c*(1)	2-8
Mixer injection signals	2-6*c*(2)	2-8
VDSP frequency selection signals	2-6*c*(5)	2-10
1-6-MHz VCO band selection signals	2-6*c*(3)	2-10
1-6-MHz VCO divisor selection signals	2-6*c*(4)	2-10
Frequency synthesizer A2	2-7	2-10
Internal synthesizer signals	2-7*b*	2-12
L.O. signal generator	2-7*e*	2-12
Master clock signal generator	2-7*c*	2-12
Pump signal generator	2-7*d*	2-12
Synthesizer outputs	2-7*a*	2-12
General	2-1	2-1
Modulator (fig. 2-2)	2-3	2-4
Power supply section	2-8	2-12
RF translator (fig. FO-4)	2-5	2-7
Transmitter 6A9/6A11 (fig. FO-2)	2-2	2-1
Control	2-2*b*	2-1
Input signals	2-2*b*(1)	2-1
ALC sample	2-2*b*(1)(*b*)	2-1
Carrier adjust	2-2*b*(1)(*d*)	2-1
Carrier enable	2-2*b*(1)(*g*)	2-3
Channel enable	2-2*b*(1)(*f*)	2-3
ISB singals	2-2*b*(1)(*i*)	2-3
TGC sample	2-2*b*(1)(*c*)	2-1
Transmitter gain control	2-2*b*(1)(*e*)	2-1
Transmitter key	2-2*b*(1)(*a*)	2-1
Tune enable	2-2*b*(1)(*h*)	2-3
Tune leveler	2-2*b*(1)(*k*)	2-3
100-kHz carrier	2-2*b*(1)(*j*)	2-3
Output signals	2-2*b*(2)	2-3
Frequency select section	2-2*d*	2-4
Frequency synthesizer (A2)	2-2*e*	2-4
Modulator	2-2*a*	2-1
Power supply	2-2*f*	2-4
RF translator	2-2*c*	2-3

General (*See* Circuit analysis, Direct maintenance, Functional description, General maintenance *and* Maintenance information).
General:

Indexes of publications	1-2	1-2

	Paragraph	Page
DA Pam 310-4	1-2*a*	1-2
DA Pam 310-7	1-2*b*	1-2
TO 0-1-31	1-2*c*	1-2
Reporting of equipment publication improvements	1-3	1-2
Scope	1-1	1-1
General maintenance:		
Frequency synthesizer adjustments	4-26	4-19
Hf VCO adjustment (fig. 4-4)	4-26*c*	4-21
RF section 2nd L.O. adjustments	4-26*d*	4-24
9.1-MHz control loop	4-26*d*(1)	4-24
90.899-MHz oscillator	4-26*d*(2)	4-24
Synthesizer bench setup procedure	4-26*a*	4-19
1-6-MHz control loop adjustments (figs. 4-2 and 4-3)	4-26*b*	4-19
Frequency synthesizer disassembly and reassembly procedure	4-27	4-26
Disassembly	4-27*a*	4-26
HF VCO	4-27*a*(4)	4-26
RF box No. 1	4-27*a*(2)	4-26
RF box No. 2	4-27*a*(3)	4-26
RF section 2nd L.O.	4-27*a*(1)	4-26
Reassembly	4-27*b*	4-27
General	4-25	4-19
Removal and replacement procedures	4-28	4-31
+6.4 Vdc power supply A10	4-28*b*	4-31
Removal	4-28*b*(1)	4-31
Replacement	4-28*b*(2)	4-31
+20 Vdc power supply A11	4-28*a*	4-31
Removal	4-28*a*(1)	4-31
Replacement	4-28*a*(2)	4-31
−28 Vdc power supply A19	4-28*c*	4-31
Removal	4-28*c*(1)	4-31
Replacement	4-28*c*(2)	4-31
General maintenance information:		
Bench testing	4-7	4-1
Blown fuses	4-12	4-2
Cable checks	4-17	4-2
Checking serviceability	4-4	4-1
Correcting trouble	4-5	4-1
Detecting faulty operation	4-2	4-1
Intermittents	4-16	4-2
Introduction	4-1	4-1
Isolating by parts substitution	4-15	4-2
Locating trouble	4-3	4-1
Parts location diagrams	4-19	4-3
Reference designation number locations	4-13	4-2
Replacing parts	4-14	4-2
Tools and test equipment	4-18	4-2
Transmitter interchangeability	4-8	4-1
Troubleshooting data	4-9	4-1
Troubleshooting techniques	4-6	4-1
Voltage and frequency measurements	4-11	4-2
Waveform analysis	4-10	4-2
General support testing:		
General	4-29	4-33

Harmonic generator (fig. FO-29) (*See* Circuit analysis).
Harmonic selector A2A2 (fig. FO-30) (*See* Circuit analysis).
Hf (pump) VCO band (preset) signals (*See* Functional description).
Hf (pump) VCO control loop A2A3A2 (fig. FO-25) (*See* Circuit analysis).
Hf (pump) VCO loop (*See* Circuit analysis).
Hf (pump) VCO preset A2A3A1 (fig. FO-26) (*See* Circuit analysis).
Hf (pump) signal generating section (*See* Circuit analysis).
Hf VCO adjustment (*See* General maintenance).
Hf (pump) VCO A2A3 (fig. FO-24) (*See* Circuit analysis).
History of equipment (*See* Maintenance information).

	Paragraph	Page
Indexes of publications (*See* General).		
Initial test equipment settings (*See* Direct support testing).		
In-lock indicator A2A3A3 (fig. FO–27) (*See* Circuit analysis).		
Input signals (*See* Functional description).		
Interconnection diagrams (*See* Maintenance information).		
Intermittents (*See* General Maintenance information *and* Maintenance information.		
Internal synthesizer signals (*See* Functional description).		
Introduction (*See* General maintenance information *and* Maintenance information).		
ISB signals (*See* Functional description).		
Isolating by parts substitution (*See* General maintenance information *and* Maintenance information).		
Isolation (*See* Maintenance information).		
Locating trouble (*See* General maintenance information *and* Maintenance information).		
Localization (*See* Maintenance information).		
Location of trouble (*See* Maintenance information).		
Logic control A2A2A1 (fig. FO–33) (*See* Circuit analysis).		
L.O. signal generating section (*See* Circuit analysis).		
L.O. signal generator (*See* Functional description).		
Low-pass filter A1A5 (*See* Circuit analysis).		
Maintenance information:		
Blown fuses	3–12	3–4
General	3–12*a*	3–4
Location of trouble	3–12*b*	3–4
Cable checks	3–17	3–7
Checking serviceability	3–4	3–1
Correcting trouble	3–5	3–1
Detecting faulty operation	3–2	3–1
Intermittents	3–16	3–6
Introduction	3–1	3–1
Isolating by parts substitution	3–15	3–6
Locating trouble	3–3	3–1
Bench troubleshooting chart	3–3*b*	3–1
Rack-mounted troubleshooting chart	3–3*a*	3–1
Parts location diagrams	3–19	3–7
Rack-mounted and bench testing	3–7	3–2
Reference designation number locations	3–13	3–5
General	3–13*a*	3–5
Table description	3–13*c*	3–5
Unit numbering system	3–13*b*	3–5
Replacing parts	3–14	3–6
Tools and test equipment	3–18	3–7
Transmitter interchangeability	3–8	3–2
Troubleshooting data	3–9	3–3
General	3–9*a*	3–3
Interconnection diagrams	3–9*d*	3–3
Parts location diagrams	3–9*f*	3–4
Resistor, capacitor, and inductor color code diagram	3–9*g*	3–4
Schematic diagrams	3–9*e*	3–3
Voltage and frequency chart	3–9*b*	3–3
Waveform illustrations	3–9*c*	3–3
Troubleshooting techniques	3–6	3–2
History of equipment	3–6*a*	3–2
Isolation	3–6*e*	3–2
Localization	3–6*d*	3–2
Preliminary examination	3–6*b*	3–2
Sectionalization	3–6*c*	3–2
Testing after repairs	3–6*f*	3–2
Voltage and frequency measurements	3–11	3–4
Waveform analysis	3–10	3–4
Master clock signal generating section (*See* Circuit analysis).		
Master clock signal generator (*See* Functional description).		
Mixer injection signals (*See* Functional description).		
Modulator (*See* Functional description).		

Paragraph Page

Modulator analysis (*See* Circuit analysis).
Multiplex carrier generator A9 (*See* Circuit analysis).

Oscillator, 90.899 MHz (*See* General maintenance).
Output signals (*See* Functional description).
Parts location diagrams (*See* General maintenance information *and* Maintenance information.
Phase-lock loop A2A6A2 1–6 MHz (fig. FO–36) (*See* Circuit analysis).
Physical test and inspection (*See* Troubleshooting at general support *and* Direct support).
Power supply analysis (fig. FO–5) (*See* Circuit analysis).
Power supply section (*See* Functional description).
Power supply A10 adjustment (*See* Direct maintenance).
Power supply A11 adjustment (*See* Direct maintenance).
Power supply PS–1 (−28 Vdc) A19 (fig. 2–12) (*See* Circuit analysis).
Power supply PS–2 (+20 Vdc) A11 (fig. FO–44) (*See* Circuit analysis).
Power supply PS–3 (+6.4 Vdc) A10 (fig. FO–45) (*See* Circuit analysis).
Preamplifier A1A1 (*See* Circuit analysis).
Preliminary examination (*See* Maintenance information).
Pump signal generator (*See* Functional description).

Rack-mounted and bench testing (*See* Maintenance information).
Rack-mounted transmitter performance test (*See* Direct support testing).
Rack-mounted troubleshooting (*See* Troubleshooting at direct support).
Rack-mounted troubleshooting chart (*See* Maintenance information).
Reference data (*See* Troubleshooting at general support *and* Direct support).
Reference designation number locations (*See* General maintenance information *and* Maintenance information).
Removal and replacement of frequency synthesizer A2 (*See* Direct maintenance).
Removal and replacement of PC cards (*See* Direct maintenance).
Removal and replacement procedures of power supply A10 (*See* General maintenance).
Removal and replacement procedures of power supply A11 (*See* General maintenance).
Removal and replacement procedures of power supply A19 (*See* General maintenance).
Removal and replacement of RF translator A1 (*See* Direct maintenance).
Removal and replacement of transmitter chassis (6A9/6A11) (*See* Direct maintenance).
Replacing parts (*See* General maintenance information *and* Maintenance information).
Reporting of equipment publication improvements (*See* General).
Resistor, capacitor, and inductor color code diagram (*See* Maintenance information).
RF box No. 1 A2A5 and RF box No. 2 A2A6 (figs. FO–41 and FO–42) (*See* Circuit analysis).
RF section 2nd L.O. adjustments (*See* General maintenance).
RF translator (*See* Functional description).
RF translator A1 analysis (*See* Circuit analysis).

Schematic diagrams (*See* Maintenance information).
Second L.O. RF section A2A4 (figs. FO–37 and FO–38) (*See* Circuit analysis).
Second L.O. variable divider A2A5A2 (figs. FO–39 and FO–40) (*See* Circuit analysis).
Sectionalization (*See* Maintenance information).
Signal control card A5 ALC and TGC alignment (*See* Direct maintenance).
Signal control card A5 AM level adjustment (*See* Direct maintenance).
Signal control A5 PC card (*See* Circuit analysis).
Signal control card A5, −20 Vdc adjustment (*See* Direct maintenance).
Synthesizer bench setup procedure (*See* General maintenance).
Synthesizer outputs (*See* Functional description).
Tables:
Adjustment and alignment procedures (table 3–11).
Automatic channel loading, bench performance test (table 3–21).
Automatic load control (ALC), bench performance test (table 3–20).
Automatic load control (ALC), performance standard test (table 3–15).
Band control card A16 signal inputs (table 3–8).

	Paragraph	Page
Band control card A16 signal outputs (table 3-9).		
Code conversion matrix cards A17 and A18 signal inputs and outputs (table 3-10).		
Control loop frequencies, bands, ranges and divider ratios (table 2-5).		
Cross-reference of circuit block numbers to reference designations (table 3-1).		
Direct support maintenance test equipment (table 3-4).		
Equipment characteristics (table 1-1).		
Frequency control code (table 2-1).		
Frequency synthesizer, bench performance test (table 3-24).		
Frequency synthesizer A2 L.O. frequency digit checks (table 3-6).		
Frequency synthesizer A2 pump frequency checks (table 3-5).		
Frequency tuning range, bench performance test (table 3-19).		
Frequency tuning range, performance standard test (table 3-13).		
Front panel controls, bench performance test (table 3-23).		
Front panel controls, performance standard test (table 3-16).		
General support maintenance test equipment (table 4-2).		
Organization of frequency synthesizing circuits (table 2-4).		
Power output adjustment, bench performance test (table 3-18).		
Power output, performance standard test (table 3-14).		
Printed circuit card adjustments (table 3-12).		
Reference designation number locations (table 3-2).		
Special tools for direct support (table 3-3).		
Special tools for general support (table 4-1).		
Transmit gain control, bench performance test (table 3-22).		
Transmit gain control, performance standard test (table 3-17).		
Variable divider synthesizer pump data (table 2-2).		
VDSP timing chart No. 1 (table 2-6).		
VDSP timing chart No. 2 (table 2-7).		
Voltage and frequency measurements (table 3-7).		
3-6-MHz oscillator band selection data (table 2-3).		
Table description (*See* Maintenance information).		
Tabulated data (*See* Description and data).		
Test connections and conditions (*See* Direct support testing).		
Test equipment and materials (*See* Direct support testing).		
Testing after repairs (*See* Maintenance information).		
TGC card A4 alignment (*See* Direct maintenance).		
TGC sample (*See* Functional description).		
Tools and test equipment (*See* General maintenance information *and* Maintenance information).		
Transmitter gain control (*See* Functional description).		
Transmit gain control A4 PC card (*See* Circuit analysis).		
Transmitter interchangeability (*See* General maintenance information *and* Maintenance information).		
Transmitter key (*See* Functional description).		
Transmitter 6A9/6A11 (*See* Functional description).		
Troubleshooting at direct support:		
General	3-20	3-7
Physical test and inspection	3-22	3-8
Reference data	3-21	3-8
Troubleshooting test conditions	3-24	3-9
Bench troubleshooting	3-24*b*	3-17
Rack-mounted troubleshooting	3-24*a*	3-9
Voltage and frequency measurements	3-25	3-34
Waveforms (figs. 3-3 and 3-4)	3-26	3-43
Troubleshooting at general support:		
General	4-20	4-3
Physical test and inspection	4-22	4-3
Reference data	4-21	4-3
Troubleshooting test conditions	4-24	4-3
Use of troubleshooting charts	4-23	4-3
Troubleshooting data (*See* General maintenance information *and* Maintenance information).		
Troubleshooting techniques (*See* General maintenance information *and* Maintenance information).		

Paragraph Page

Troubleshooting test conditions. (*See* Troubleshooting at general support *and* Direct support).
Tune enable (*See* Functional description).
Tune leveler (*See* Functional description).

Unit numbering system (*See* Maintenance information).
Use of troubleshooting charts (*See* Troubleshooting at general support).

Variable divider-synthesizer pump A2A6A1 (fig. FO-35) (*See* Circuit analysis).
VCO A2A7 1-6 MHz (fig. FO-34) (*See* Circuit analysis).
VCO band selection signals, 1-6 MHz (*See* Functional description).
VCO divisor selection signals, 1-6 MHz (*See* Functional description).
VCO loop 1-6 MHz (*See* Circuit analysis).
VDSP frequency selection signals (*See* Functional description).
Video amplifier A1A3 (*See* Circuit analysis).
Video amplifier and mixer A2A2A3 (fig. FO-32) (*See* Circuit analysis).
Voltage and frequency chart (*See* Maintenance information).
Voltage and frequency measurements (*See* General maintenance information, Maintenance information *and* Troubleshooting at direct support).
Voltage regulator A1A6, −7 Vdc (*See* Circuit analysis).
Waveform analysis (*See* General maintenance information *and* Maintenance information).
Waveform illustrations (*See* Maintenance information).
Waveforms (*See* Troubleshooting at direct support).

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LEAD (7)
ATAD (5)
USA Dep (1)
Sig Sec USA Dep (3)
Sig Dep (3)
Sig FLDMS (1)
Ft Richardson (ECOM Ofc) (2)
USASCS (100)
Units org under fol TOE:
(1 copy each unit)
11-158
29-134
29-136

NG: None.
USAR: None.
For explanation of abbreviations used, see AR 310-50.

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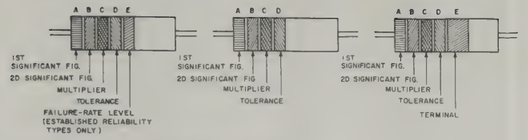
TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY CB	0	0	1			±20%	±20%		A			$-55°_{TO}+70°C$	10-55 Hz
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				$-55°_{TO}+85°C$	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				$-55°_{TO}+125°C$	10-2,000Hz
GREEN		5	5		±5%				F			500		
BLUE		6	6										$-55°_{TO}+150°C$	
PURPLE (VIOLET)		7	7											
GREY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN				±10%	±10%	±10%	±10%						

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		± 2.0 UUF	CC
BROWN	−30	1	1	10	± 1%		
RED	−80	2	2	100	±2 %	± 0.25 UUF	
ORANGE	−150	3	3	1,000			
YELLOW	−220	4	4				
GREEN	−330	5	5		± 5 %	± 0.5 UUF	
BLUE	−470	6	6				
PURPLE (VIOLET)	−750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	± 10%		
GOLD	+100					± 1.0 UUF	
SILVER							

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY)			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	SILVER	8	SILVER	0.01					
WHITE	9	GOLD	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

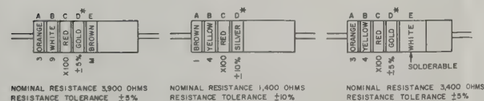
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

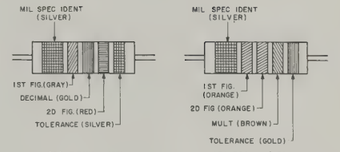
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



COLOR CODING FOR TUBULAR ENCAPSULATED R.F CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED

TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R F CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.

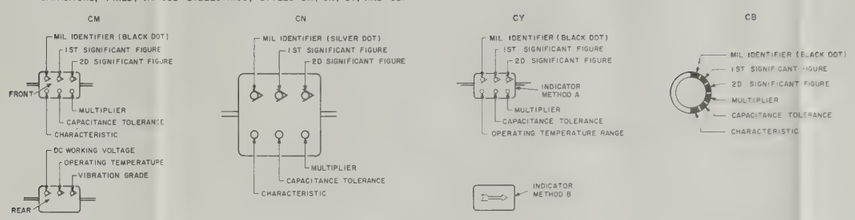


TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB

COLOR	MIL CHAR	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE				CHARACTERISTIC				DC WORKING VOLTAGE	OPERATING TEMP RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CY	CB	CM	CY, CM	CM
BLACK	CM, CY, CB	0	0	1			±20%	±20%	A					-55° TO +70°	0-55 H z
BROWN		1	1	10				B	E	B					
RED		2	2	100	±2%		±2%	±2%	C					-55° TO +85°	
ORANGE		3	3	1,000		±1%						D	300		
YELLOW		4	4	10,000					F					-55° TO +125°	0-2,000 HZ
GREEN		5	5	100,000	±1%				F				500		
BLUE		6	6											-55° TO +150°	
PURPLE (VIOLET)		7	7												
GREY		8	8												
WHITE		9	9												
GOLD				0.1			+100% -0%	±5%							
SILVER				0.01	±10%	±10%	±10%	±10%							

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

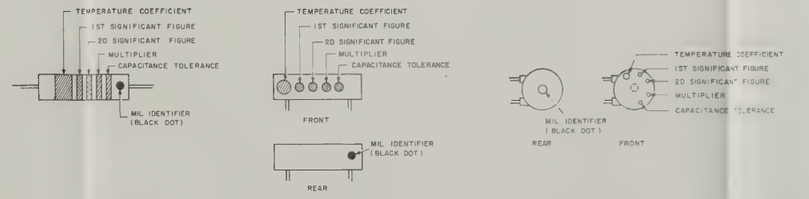
COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG	2D SIG FIG	MULTIPLIER	CAPACITANCE TOLERANCE		MIL CHAR
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GREY		8	8	0.01			
WHITE		9	9		±10%		
GOLD	-100					±1.0 UUF	
SILVER							

1 THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.

2 LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS MIL-C-5, MIL-C-250, MIL-C-11272B, AND MIL-C-39000C RESPECTIVELY.

3 LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-STD-202C.

4 TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.



C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS

ESC-FM 1794-71

Figure FO-1. Color code marking for MIL-STD resistors, capacitors, and inductors.

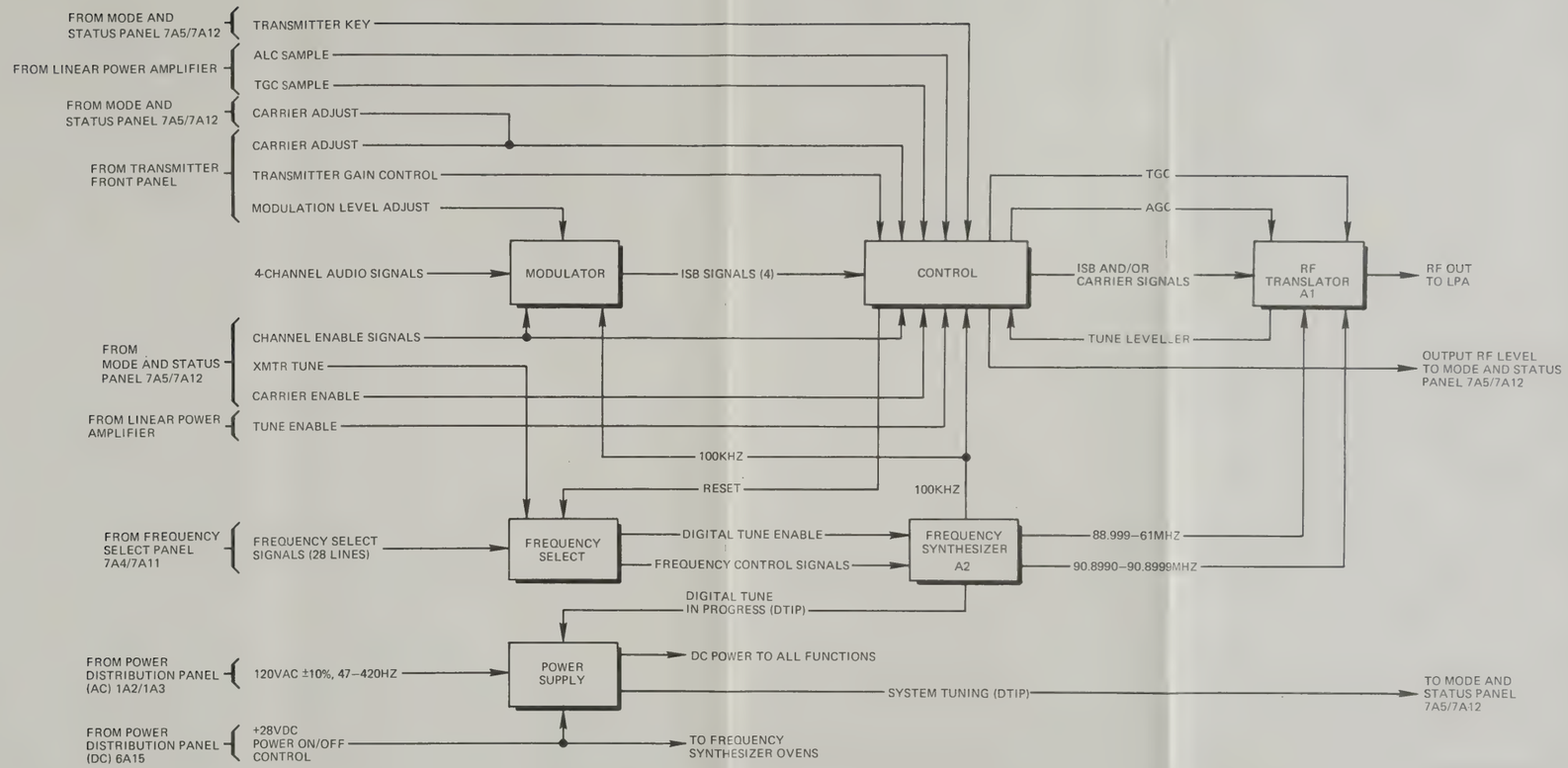


Figure FO-2. Transmitter 6A9/6A11, block diagram.

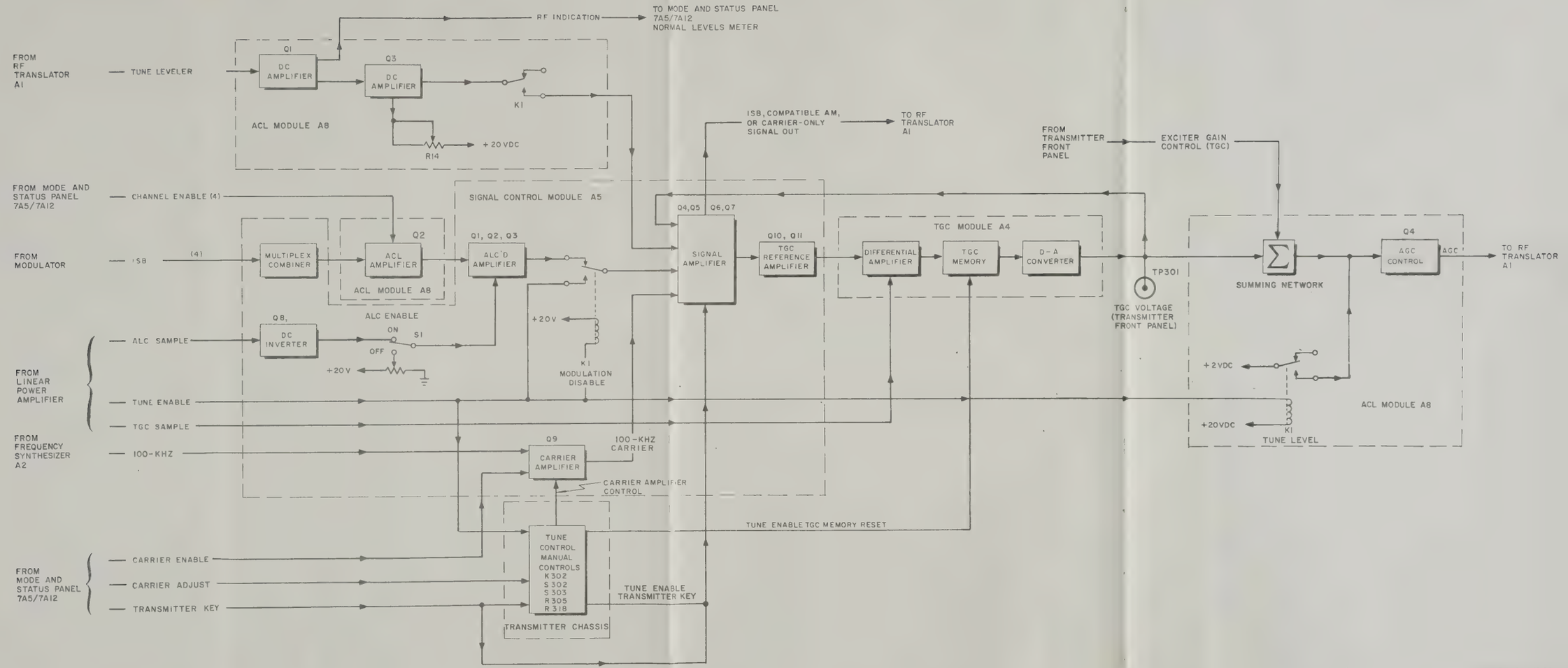


Figure FO-3. Control section, block diagram.

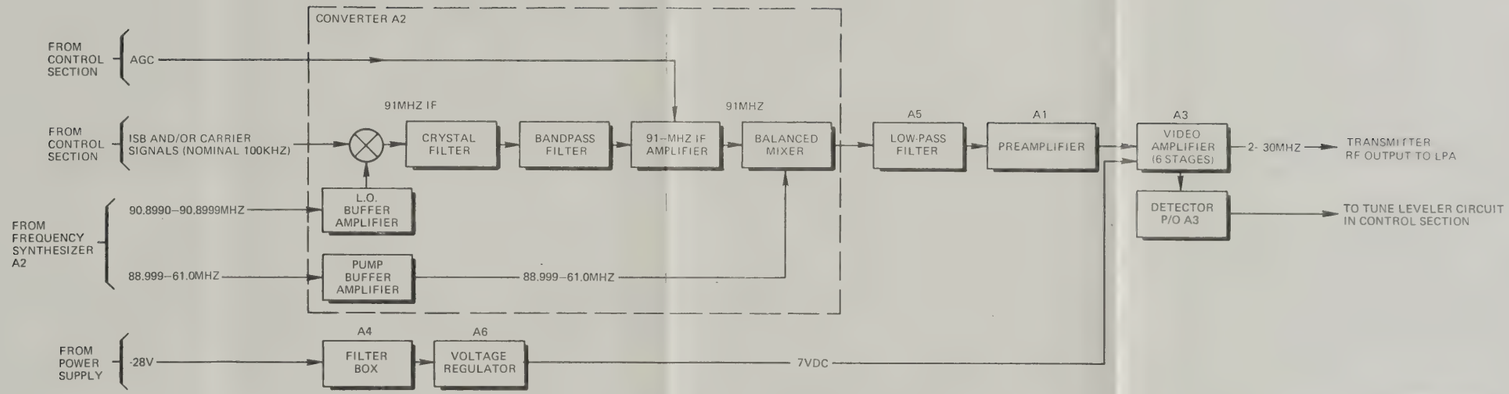


Figure FO-4. RF translator A1, block diagram.

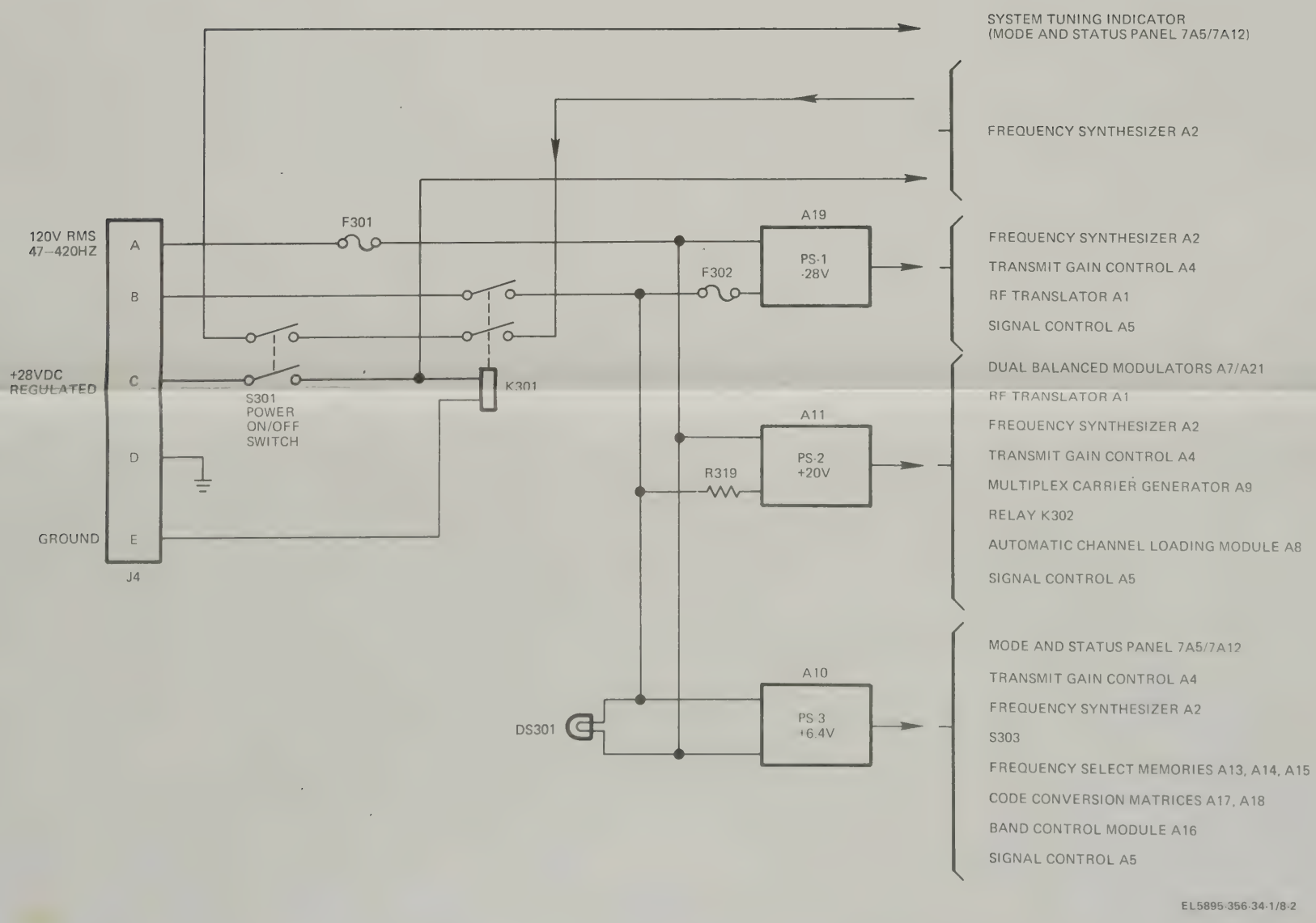
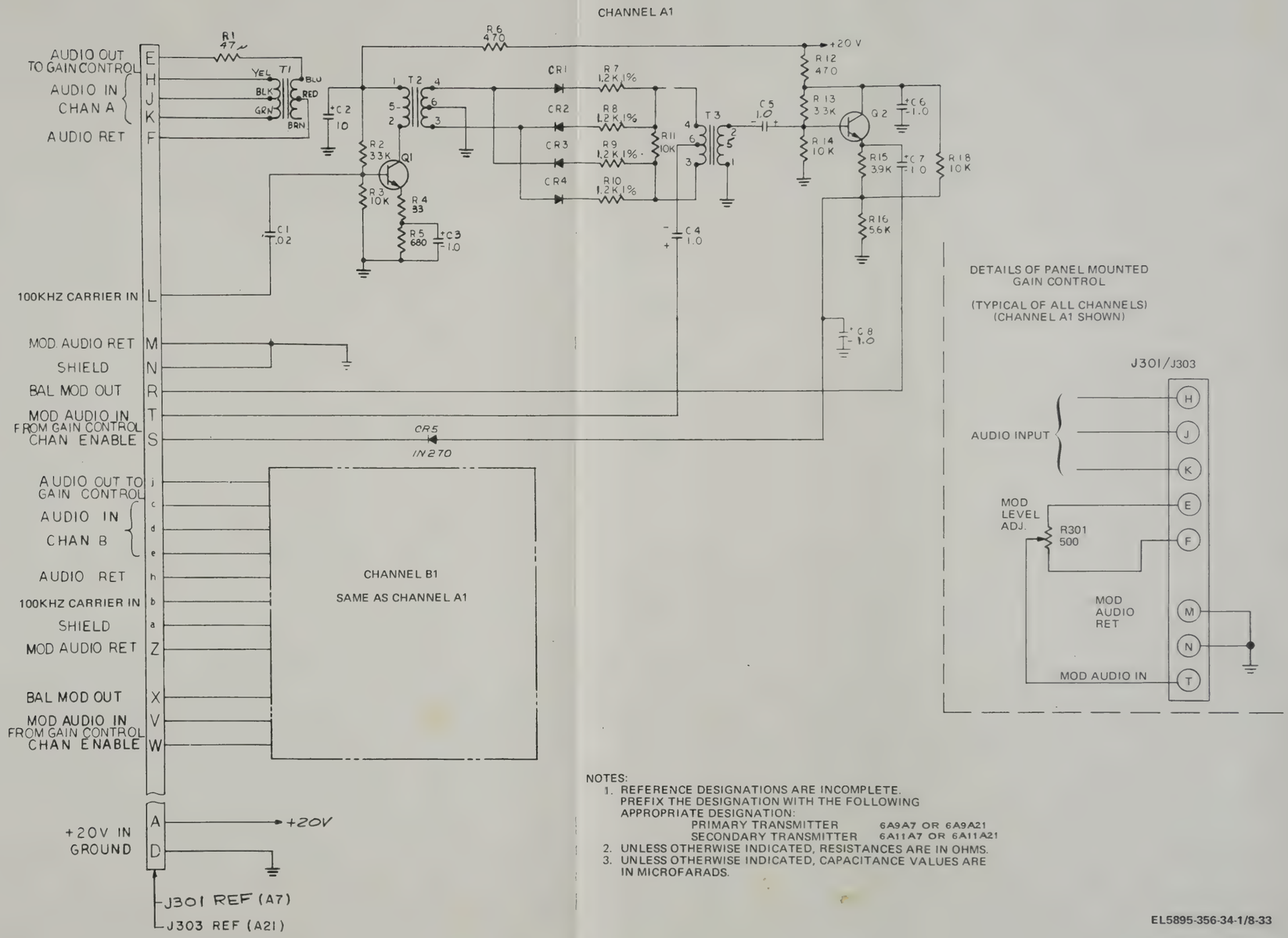


Figure FO–5. Power supply section, block diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A7 OR 6A9A21
   SECONDARY TRANSMITTER 6A11A7 OR 6A11A21
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS.

EL5895-356-34-1/8-33

Figure FO-6. Dual balanced modulator A7/A21, schematic diagram.

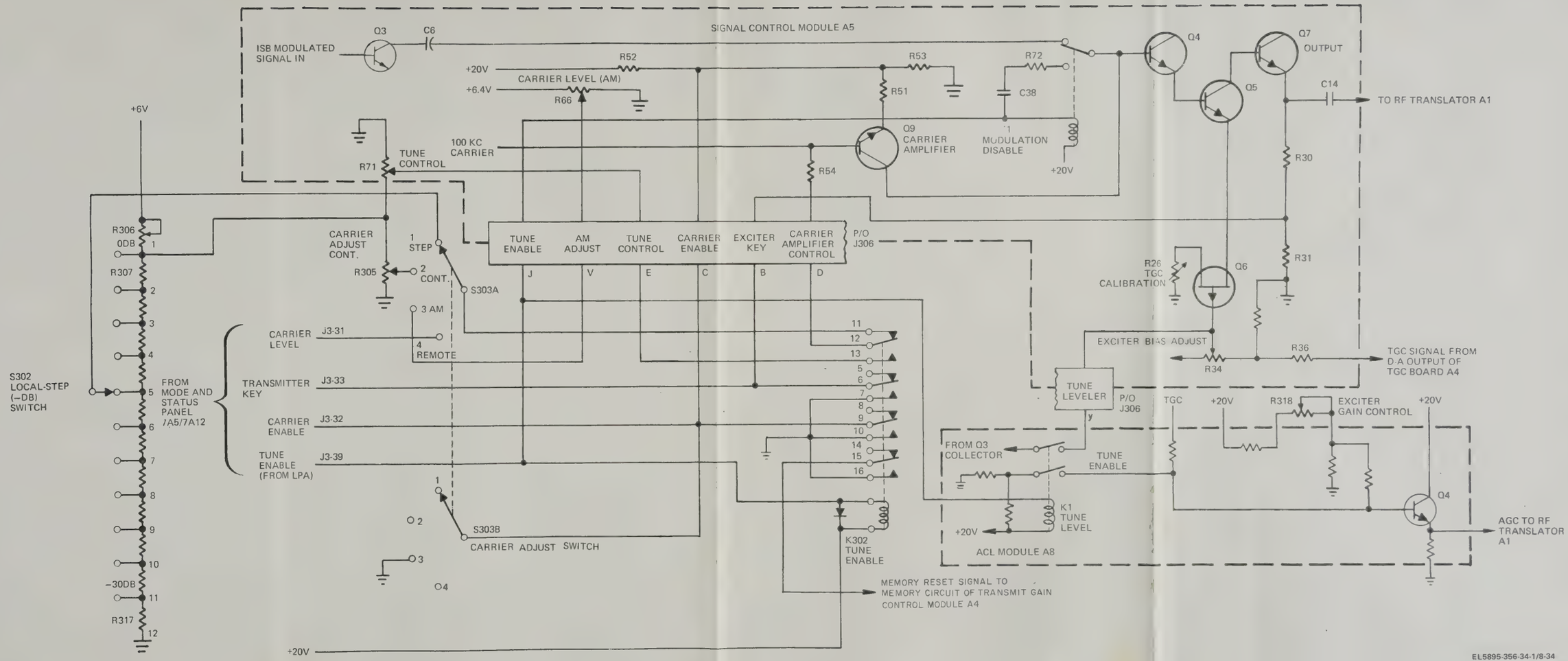


Figure FO–7. Control circuits, simplified schematic diagram.

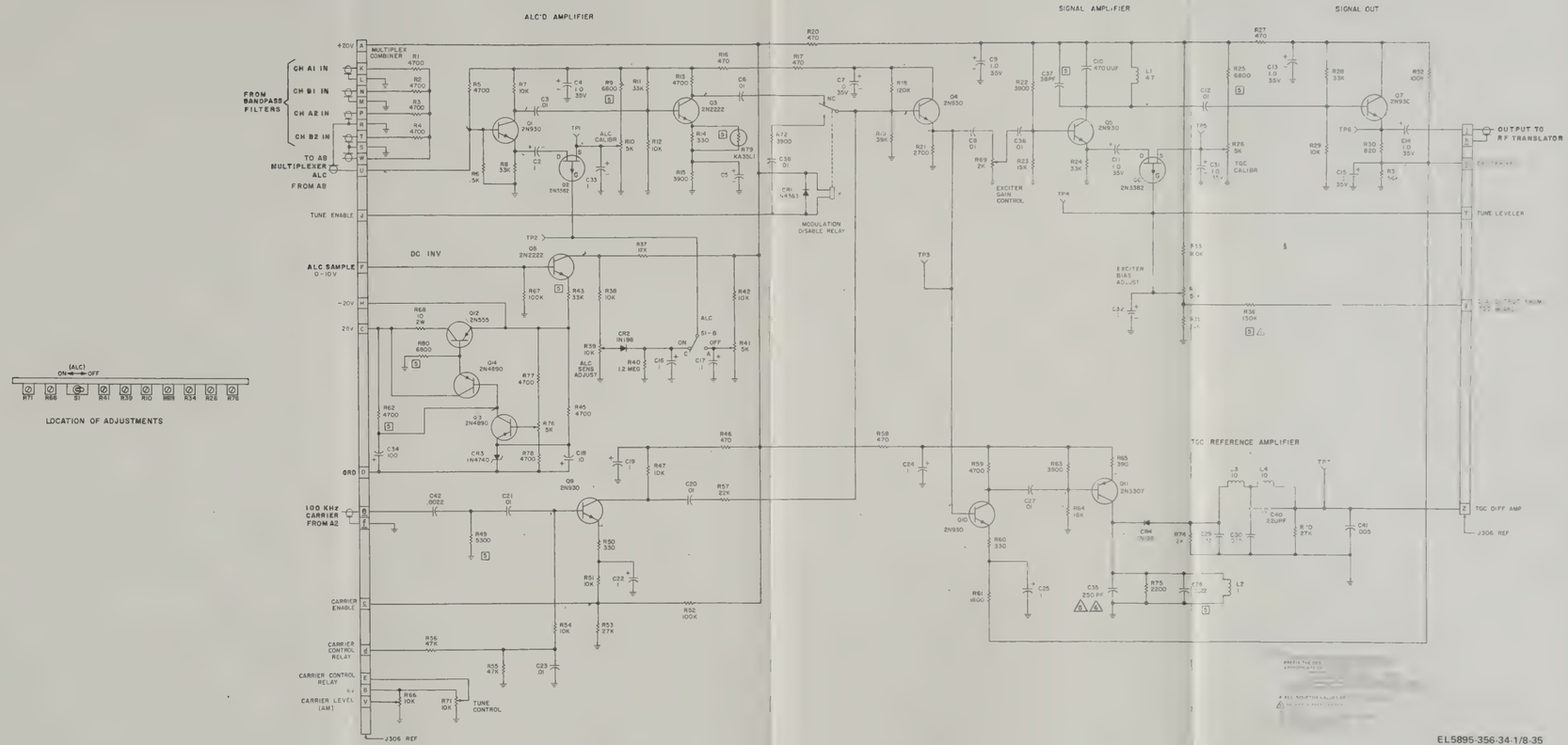


Figure FO-8. Signal control A5, schematic diagram.

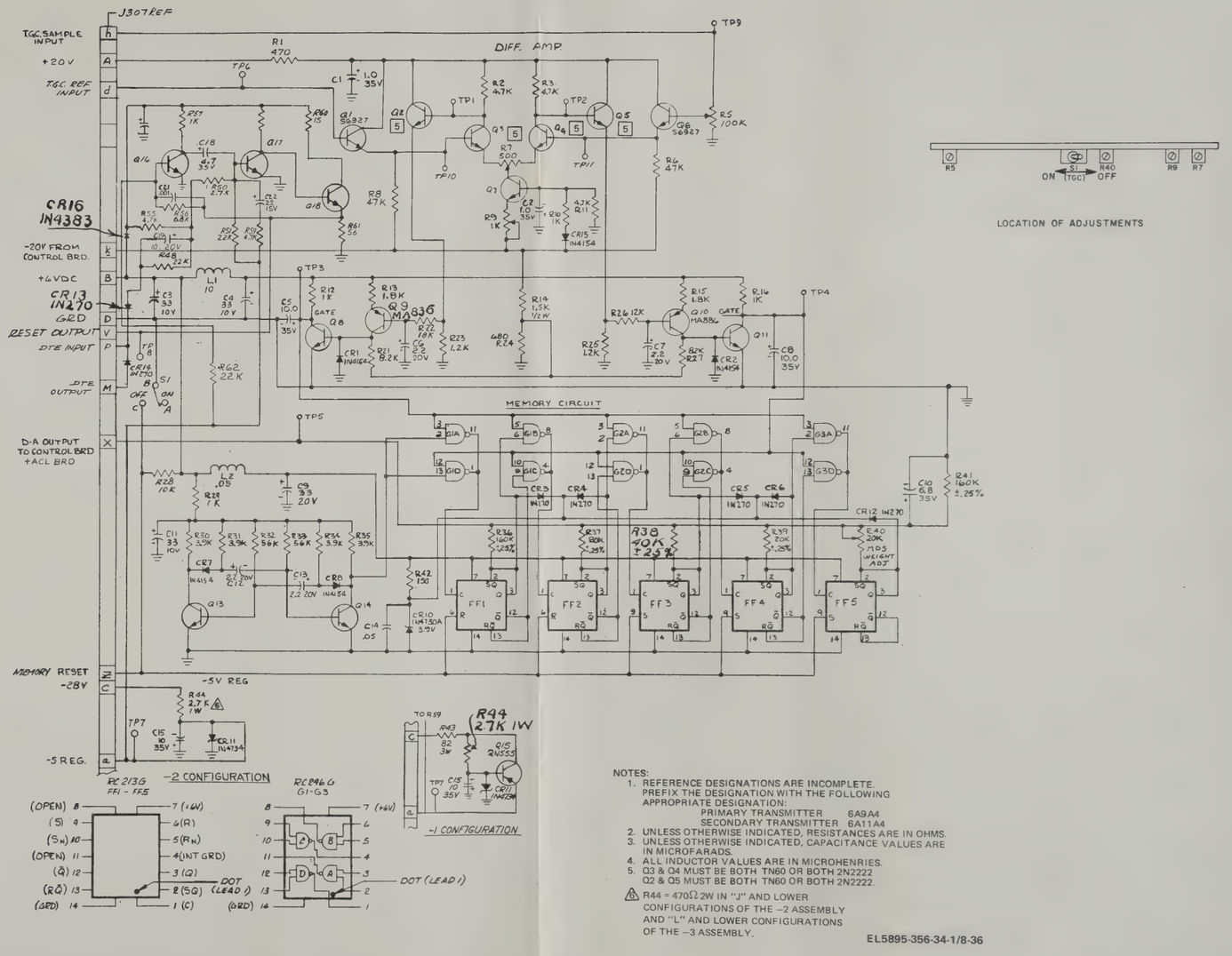
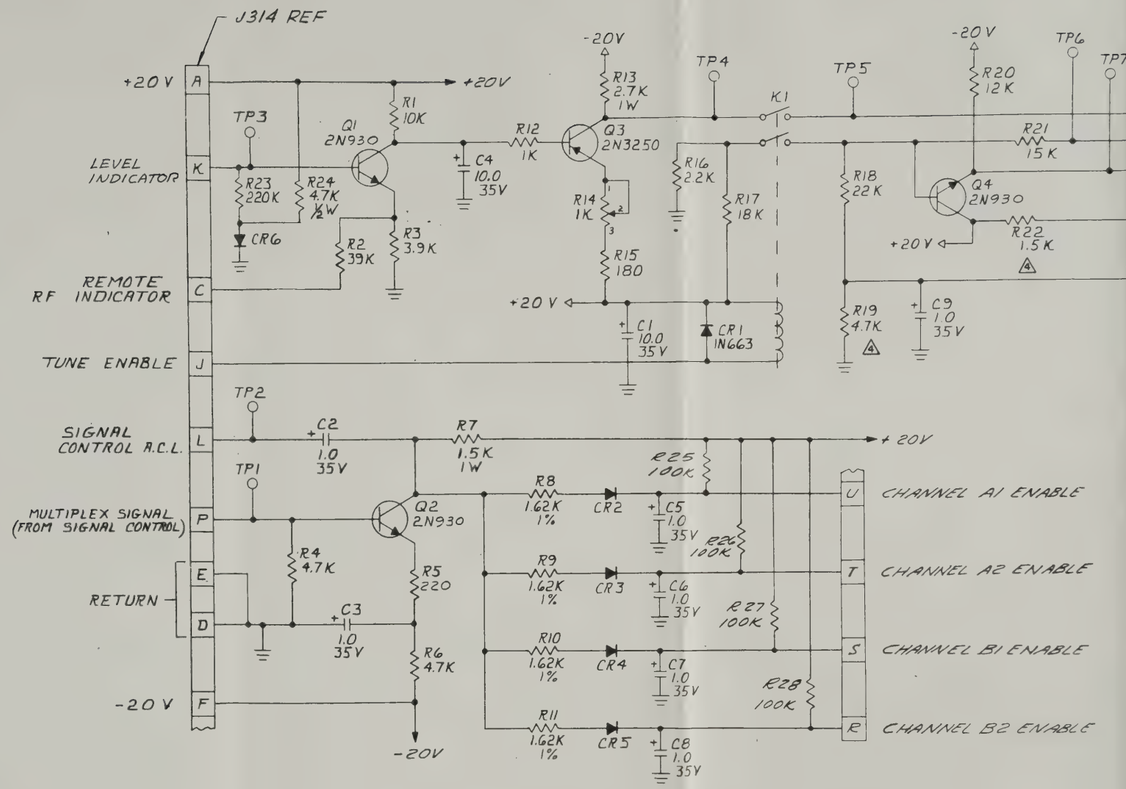
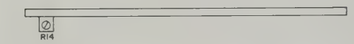


Figure FO–9. Transmit gain control A4, schematic diagram.





LOCATION OF ADJUSTMENTS

NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A8
   SECONDARY TRANSMITTER 6A11A8
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS.
4. SELECT IN TEST, CENTER VALUE SHOWN.
5. UNLESS OTHERWISE INDICATED, ALL DIODES ARE 1N4154.

EL5895-356-34-1/8-37

Figure FO–10. Automatic channel loading A8, schematic diagram.

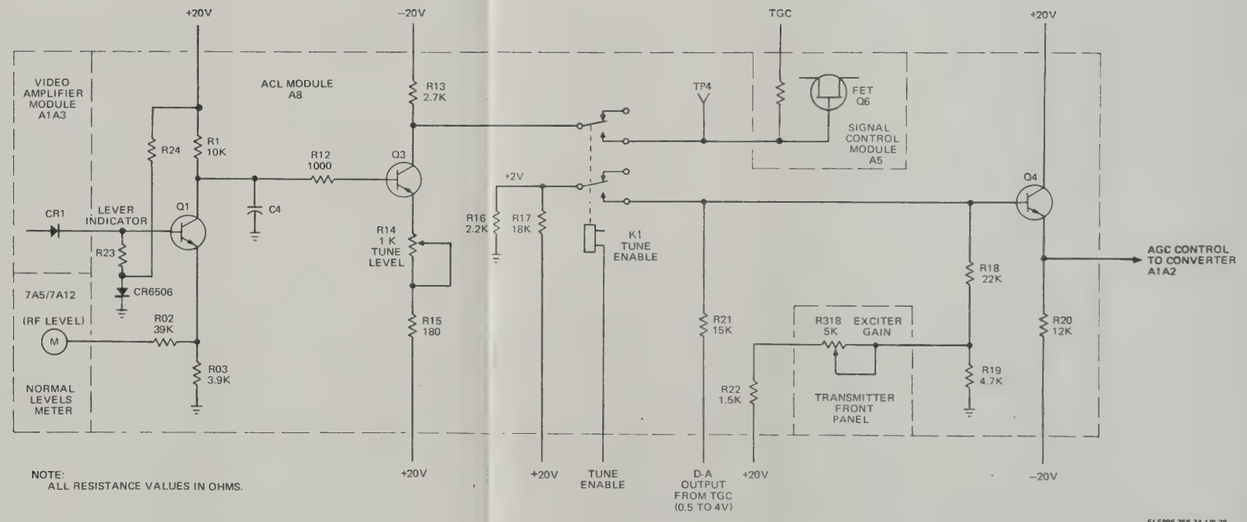
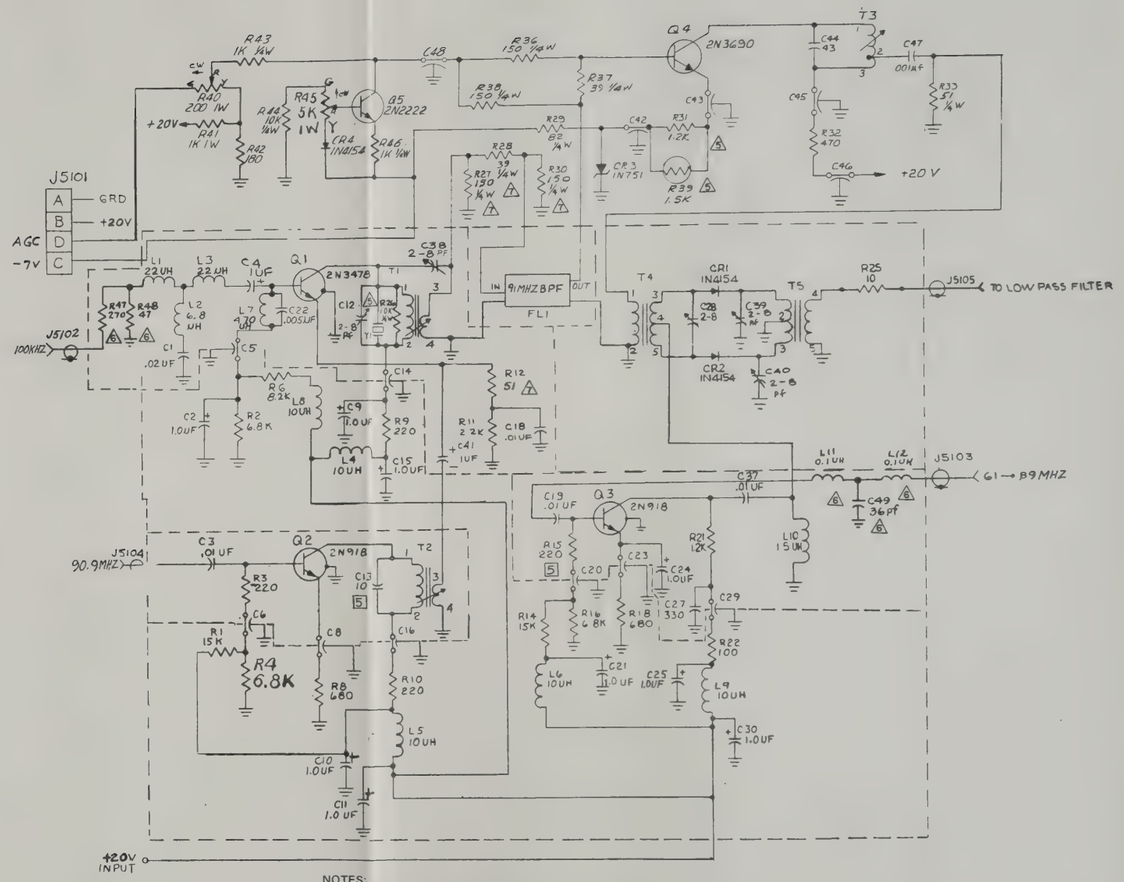


Figure FO–11. Tune leveler circuits, simplified schematic diagram.



NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A1A2
   SECONDARY TRANSMITTER 6A11A1A2
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN PICOFARADS.
4. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.

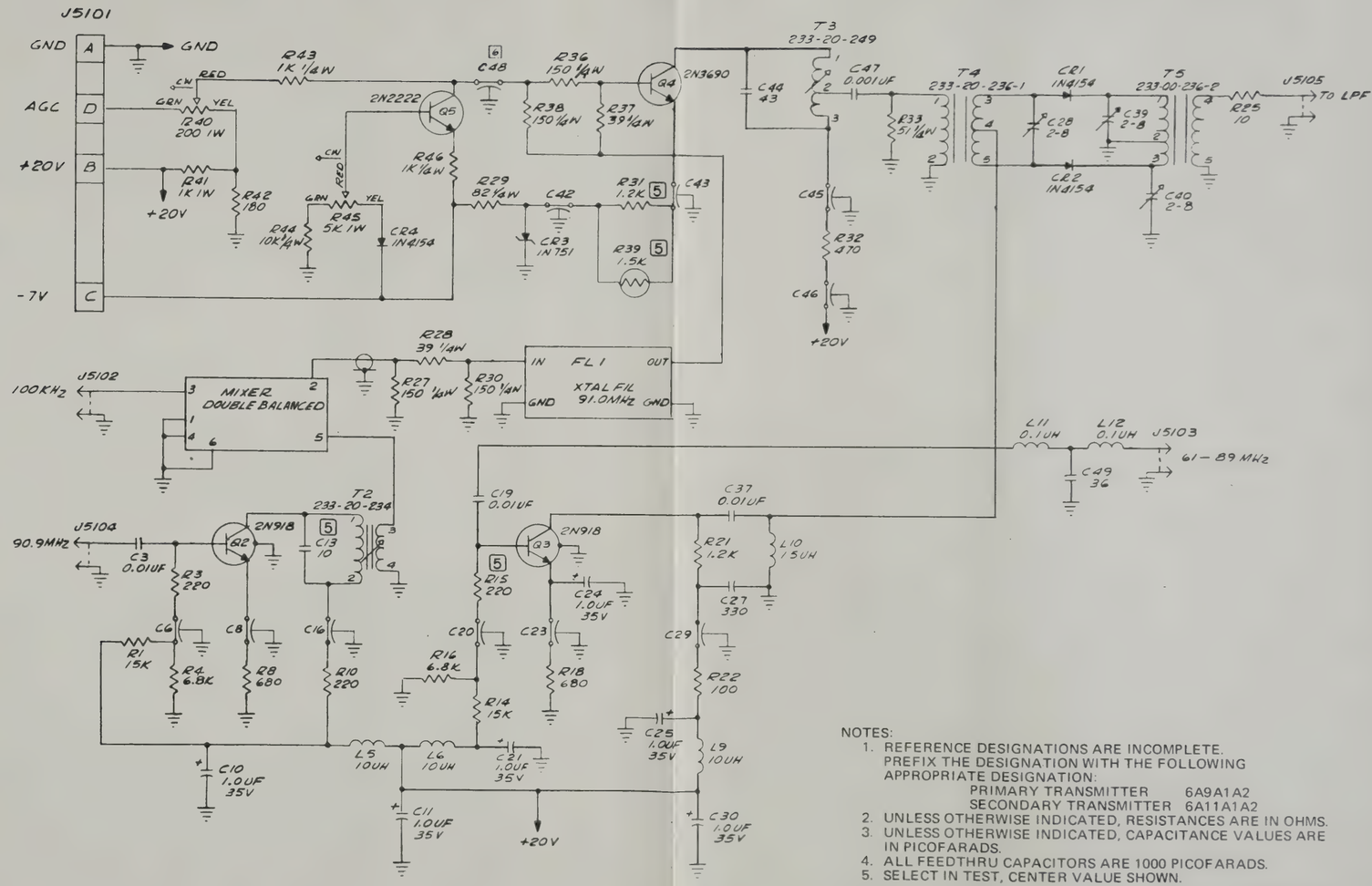
⚠5 SELECT IN TEST, CENTER VALUE SHOWN.

⚠6 COMPONENT NOT PRESENT IN "A" CONFIGURATION.

⚠7 IN "A" CONFIGURATION R12 = 100Ω, R27 = 330Ω, R28 = 18Ω, AND R30 = 330Ω.

EL5895-356-34-1/8-39

Figure FO–12. Converter A1A2, (230–20–255) schematic diagram.

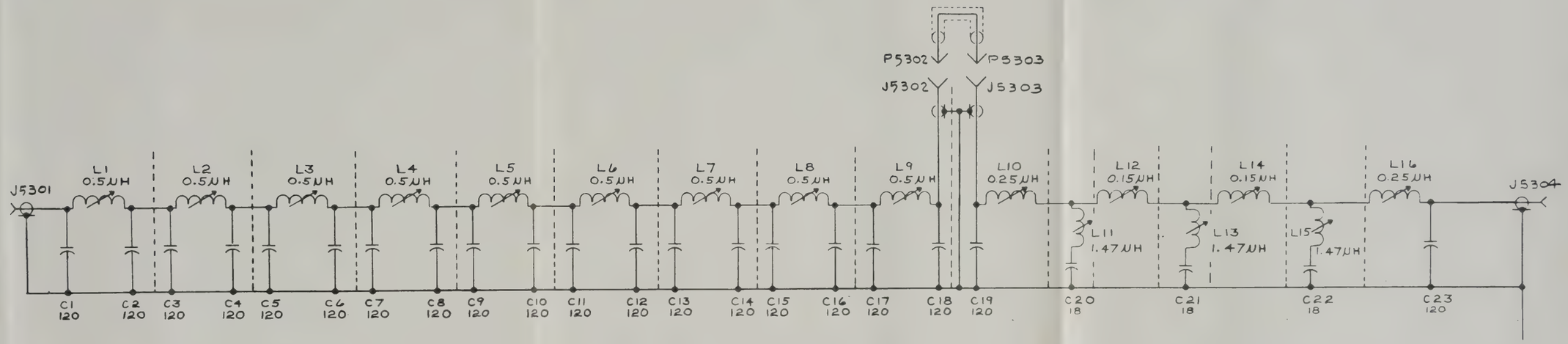


NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A1A2
   SECONDARY TRANSMITTER 6A11A1A2
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN PICOFARADS.
4. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.
5. SELECT IN TEST, CENTER VALUE SHOWN.

EL5895-356-34-1/8-40

Figure FO-13. Converter A1A2, (233-20-262) schematic diagram.

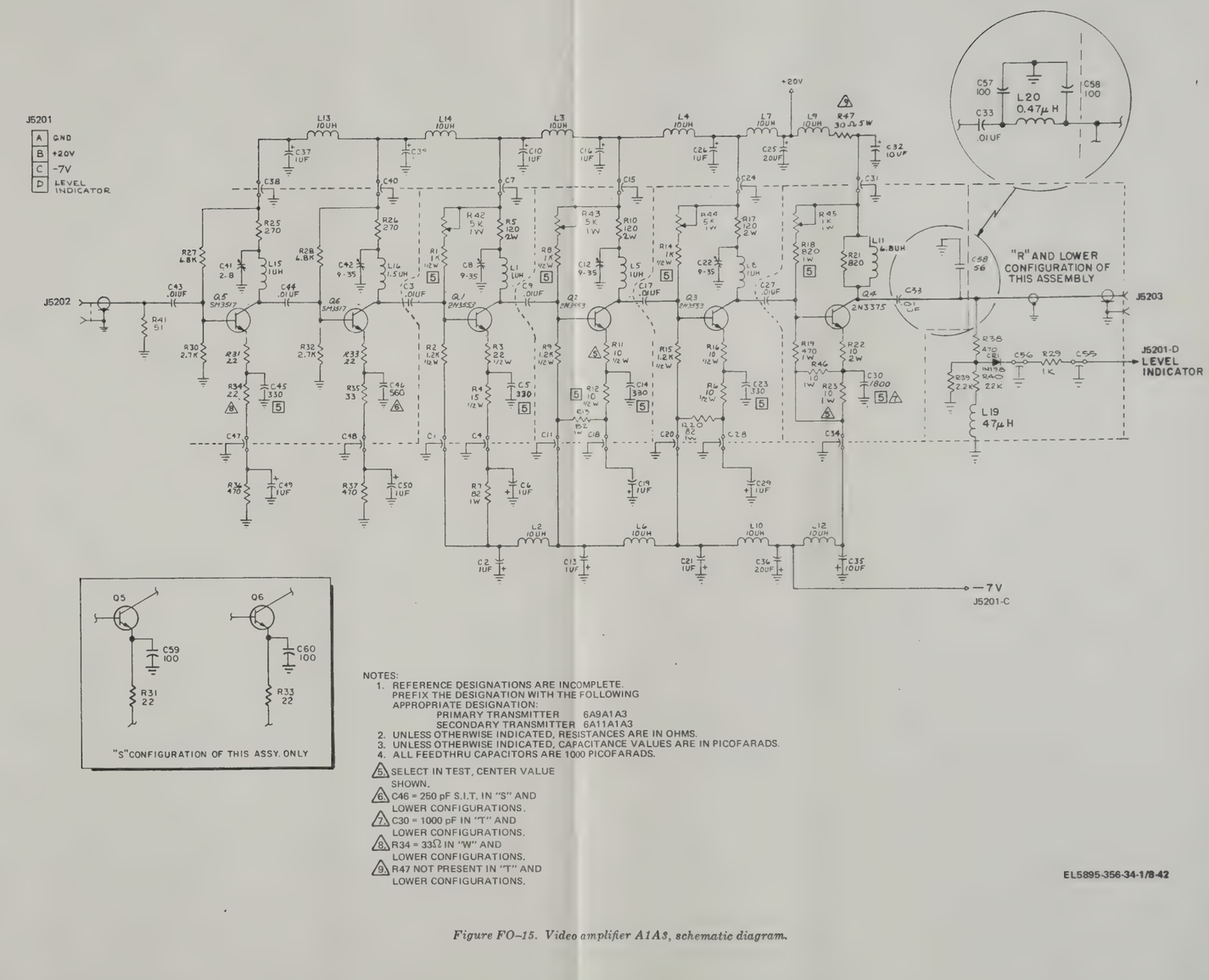


NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A1A5
   SECONDARY TRANSMITTER 6A11A1A5
2. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN PICOFARADS.

EL5895-356-34-1/8-41

Figure FO–14. Low-pass filter A1A5, schematic diagram.

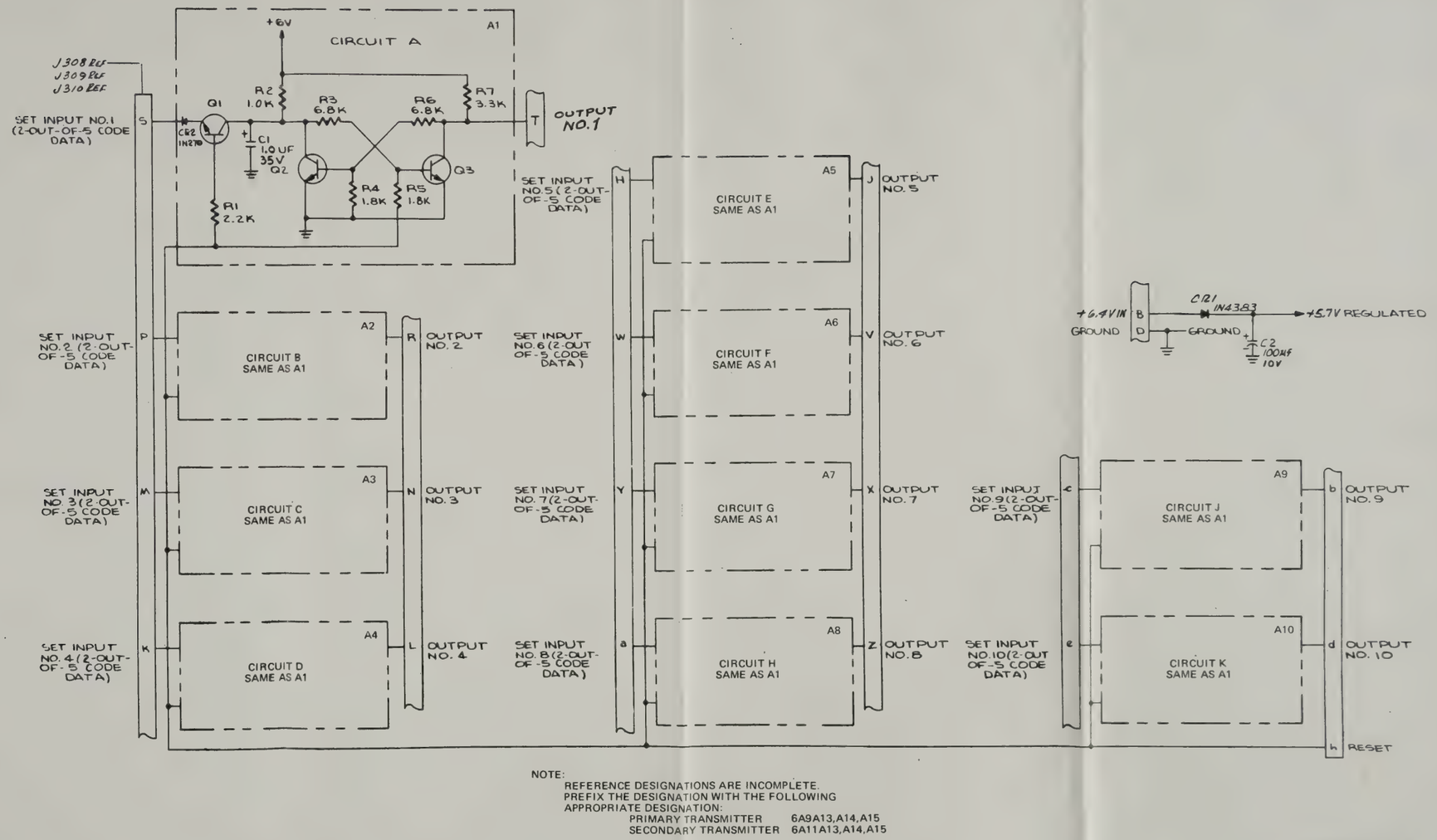


NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A1A3
   SECONDARY TRANSMITTER 6A11A1A3
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN PICOFARADS.
4. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.

5. SELECT IN TEST, CENTER VALUE SHOWN.
6. C46 = 250 pF S.I.T. IN "S" AND LOWER CONFIGURATIONS.
7. C30 = 1000 pF IN "T" AND LOWER CONFIGURATIONS.
8. R34 = 33Ω IN "W" AND LOWER CONFIGURATIONS.
9. R47 NOT PRESENT IN "T" AND LOWER CONFIGURATIONS.

EL5895-356-34-1/8-42

Figure FO–15. Video amplifier A1A3, schematic diagram.



NOTE:
REFERENCE DESIGNATIONS ARE INCOMPLETE.
PREFIX THE DESIGNATION WITH THE FOLLOWING
APPROPRIATE DESIGNATION:
PRIMARY TRANSMITTER 6A9A13,A14,A15
SECONDARY TRANSMITTER 6A11A13,A14,A15

EL5895-356-34-1/8-43

Figure FO–16. Frequency select memory A13, A14, and A15, schematic diagram.

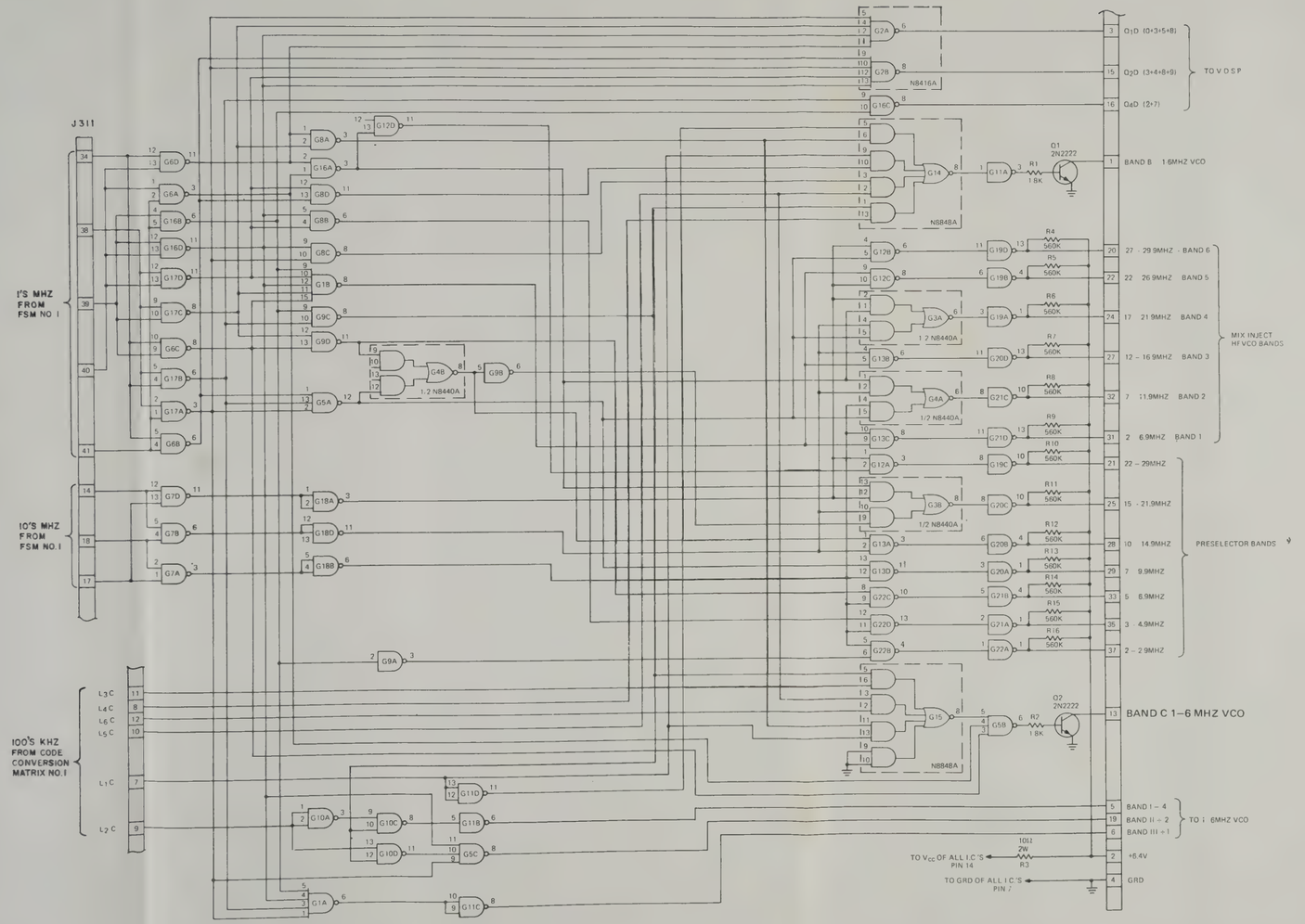


Figure FO–17. Band control A16, schematic diagram.

DIGIT	UNITS OF MHZ INPUT CODE				10'S OF MHZ INPUT CODE			100'S OF KHZ INPUT CODE FROM CONV MATRIX NO. 1				
	41	40	39	38	34	14	18	17	?	9	11	8	10	12
0	G	+V	G	G	+V	G	+V	+V	G	G	G	+V	+V	G
1	+V	+V	G	G	G	+V	+V	G	G	G	G	+V	+V	G
2	+V	G	+V	G	G	+V	G	+V	G	G	+V	G	+V	G
3	G	+V	+V	G	G				G	G	+V	G	+V	G
4	G	+V	G	+V	G				G	G	+V	G	G	+V
5	G	G	+V	+V	G				G	+V	G	G	G	+V
6	G	G	+V	G	+V				G	+V	G	G	G	+V
7	G	G	G	+V	+V				G	+V	G	G	G	+V
8	+V	G	G	+V	G				+V	+V	G	G	G	+V
9	+V	G	G	G	+V				+V	+V	G	+V	G	+V

+V = +5 +V' = +20

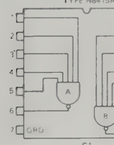
INPUTS FROM		OUTPUTS TO 1–6 MHZ VCO DIVIDER		
FREQ SEL MEM 1 AND 2	CCM NO. 1			
UNITS OF MHZ 100'S OF KHZ	L_2C	6 (−1)	19 (−2)	5 (−4)
0.0 – 1.9	G	+V	G	G
2.0 – 2.4	G	G	G	+V
2.5 – 3.9	+V	G	+V	G
4.0 – 6.9	G	+V	G	G
7.0 – 7.4	G	G	G	+V
7.5 – 8.9	+V	G	+V	G
9.0 – 9.9	G	+V	G	G

3–6MHZ OSCILLATOR BAND SELECTION DATA				
UNITS OF MHZ	100'S OF KHZ	BAND A	BAND B	BAND C
0	0-7	–	X	–
	8-9	–	–	X
1	0-9	–	–	X
2	0-1	–	X	–
	2-4	–	–	X
	5-8	X	–	–
	9	–	X	–
3	0-3	–	X	–
	4-9	–	–	X
4	0-7	X	–	–
	8-9	–	X	–
5	0-7	–	X	–
	8-9	–	–	X
6	0-9	–	–	X
7	0-1	–	X	–
	2-4	–	–	X
	5-8	X	–	–
	9	–	X	–
8	0-3	–	X	–
	4-9	–	–	X
9	0-7	X	–	–
	8-9	–	X	–

BAND A = 3.001 -3.8 MHz = NEITHER Q1 OR Q2 CONDUCTING
BAND B = 3.801 -4.8 MHz = Q1 CONDUCTING
BAND C = 4.801 -6.0 MHz = Q2 CONDUCTING

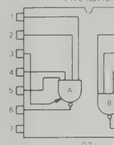
MSD FOR REQUIRED RESET			
1'S MHZ INPUT	PINS		
	16	15	3
1→6	0	0	0
2→7	1	0	0
3→8	0	1	1
4→9	0	1	0
0→5	0	0	1

TYPE N8415A



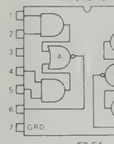
TYPE N8480A/N8889A

TYPE N8416A

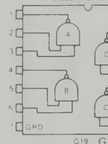


TYPE N8848A

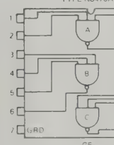
TYPE N8440A



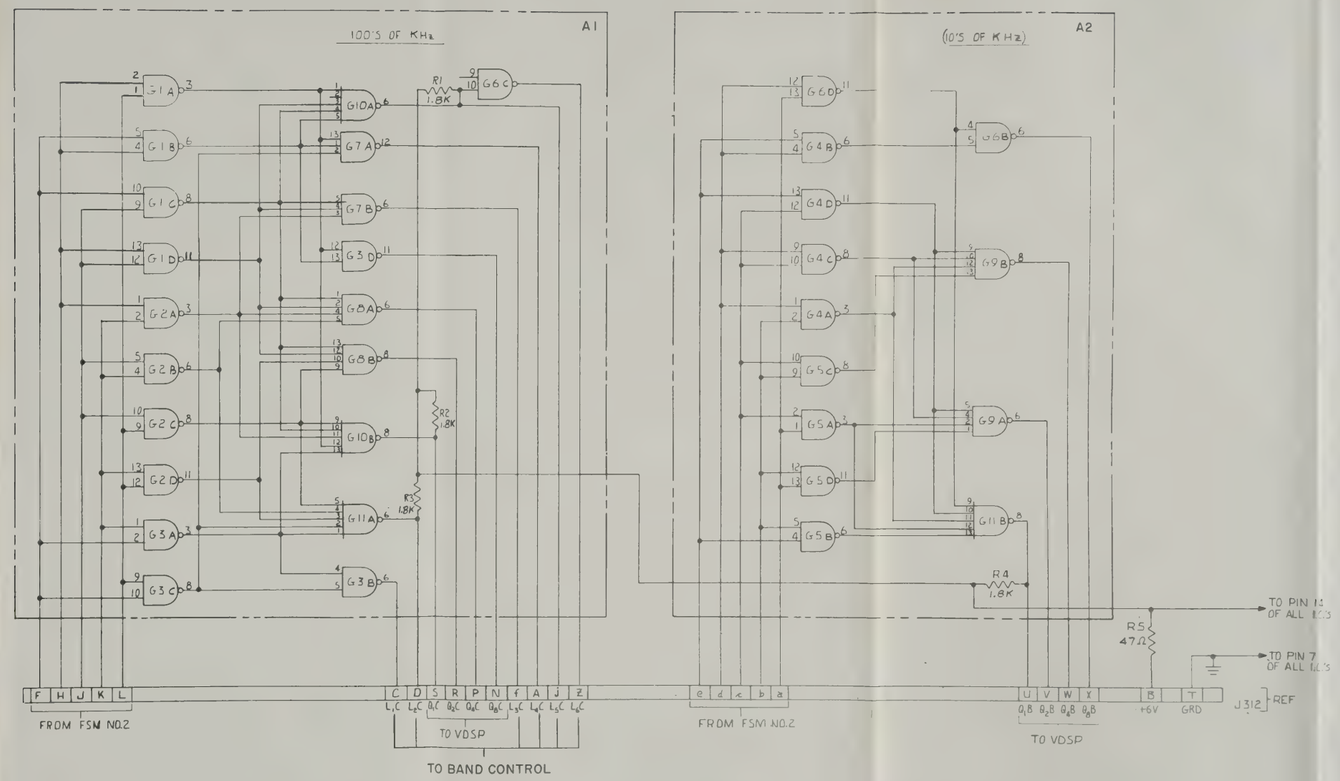
TYPE 8881A OR SN7401N

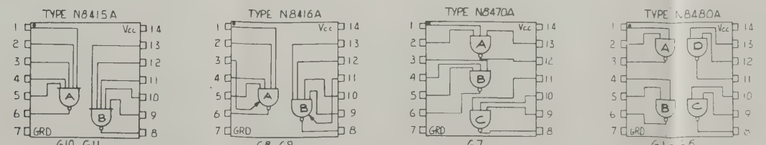


TYPE N8470A



NOTE:
REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
PRIMARY TRANSMITTER 6A9A16
SECONDARY TRANSMITTER 6A11A16



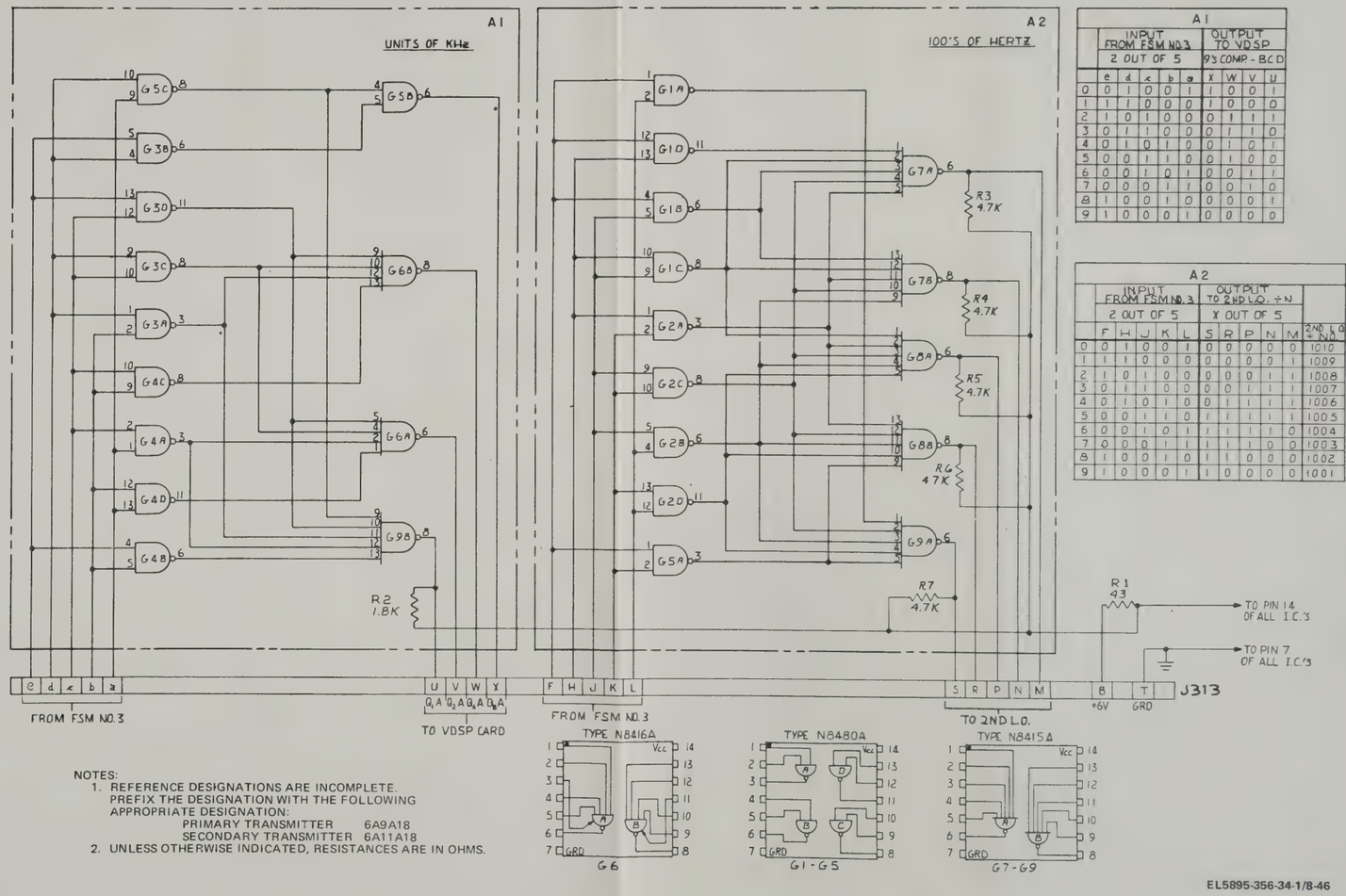


NOTE:
REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
PRIMARY TRANSMITTER 6A9A17
SECONDARY TRANSMITTER 6A11A17

	INPUT 2 OUT OF 5					OUTPUT TO VDSP 9's COMP BCD					OUTPUT TO BAND CONTROL					
	F	H	J	K	L	N	P	R	S		C	D	f	A	J	Z
A1																
A2	e	d	c	b	a	X	W	V	U		-	-	-	-	-	-
0	0	0	0	0	1	1	0	0	1		0	0	0	1	1	0
1	0	0	0	1	0	1	0	0	0		0	0	0	1	1	0
2	0	0	0	1	1	0	1	1	1		0	0	1	0	1	0
3	0	0	1	0	0	0	1	1	0		0	0	1	0	1	0
4	0	0	1	0	1	0	1	0	1		0	0	1	0	0	1
5	0	0	1	1	0	0	1	0	0		0	0	1	0	0	1
6	0	0	1	1	1	0	0	1	1		0	1	0	0	0	1
7	0	0	0	1	1	0	0	1	0		0	1	0	0	0	1
8	1	0	0	1	0	0	0	0	1		1	1	0	0	0	1
9	1	0	0	0	1	0	0	0	0		1	1	0	1	0	1

EL5895-356-34-1/8-45

Figure FO–18. Code conversion matrix No. 1 (A17), schematic diagram.



A1								
INPUT FROM FSM NO.3 2 OUT OF 5					OUTPUT TO VDSP 9's COMP - BCD			
	e	d	c	b	a	X	W	V	U
0	0	1	0	0	1	1	0	0	1
1	1	1	0	0	0	1	0	0	0
2	1	0	1	0	0	0	1	1	1
3	0	1	1	0	0	0	1	1	0
4	0	1	0	1	0	0	1	0	1
5	0	0	1	1	0	0	1	0	0
6	0	0	1	0	1	0	0	1	1
7	0	0	0	1	1	0	0	1	0
8	1	0	0	1	0	0	0	0	1
9	1	0	0	0	1	0	0	0	0

A2										
INPUT FROM FSM NO.3 2 OUT OF 5						OUTPUT TO 2ND L.O. ÷N X OUT OF 5					2ND L.O. ÷ NO.
	F	H	J	K	L	S	R	P	N	M	
0	0	1	0	0	1	0	0	0	0	0	1010
1	1	1	0	0	0	0	0	0	0	1	1009
2	1	0	1	0	0	0	0	0	1	1	1008
3	0	1	1	0	0	0	0	1	1	1	1007
4	0	1	0	1	0	0	1	1	1	1	1006
5	0	0	1	1	0	1	1	1	1	1	1005
6	0	0	1	0	1	1	1	1	1	0	1004
7	0	0	0	1	1	1	1	1	0	0	1003
8	1	0	0	1	0	1	1	0	0	0	1002
9	1	0	0	0	1	1	0	0	0	0	1001

NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A18
   SECONDARY TRANSMITTER 6A11A18
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.

EL5895-356-34-1/8-46

Figure FO–19. Code conversion matrix No. 2 (A18), schematic diagram.

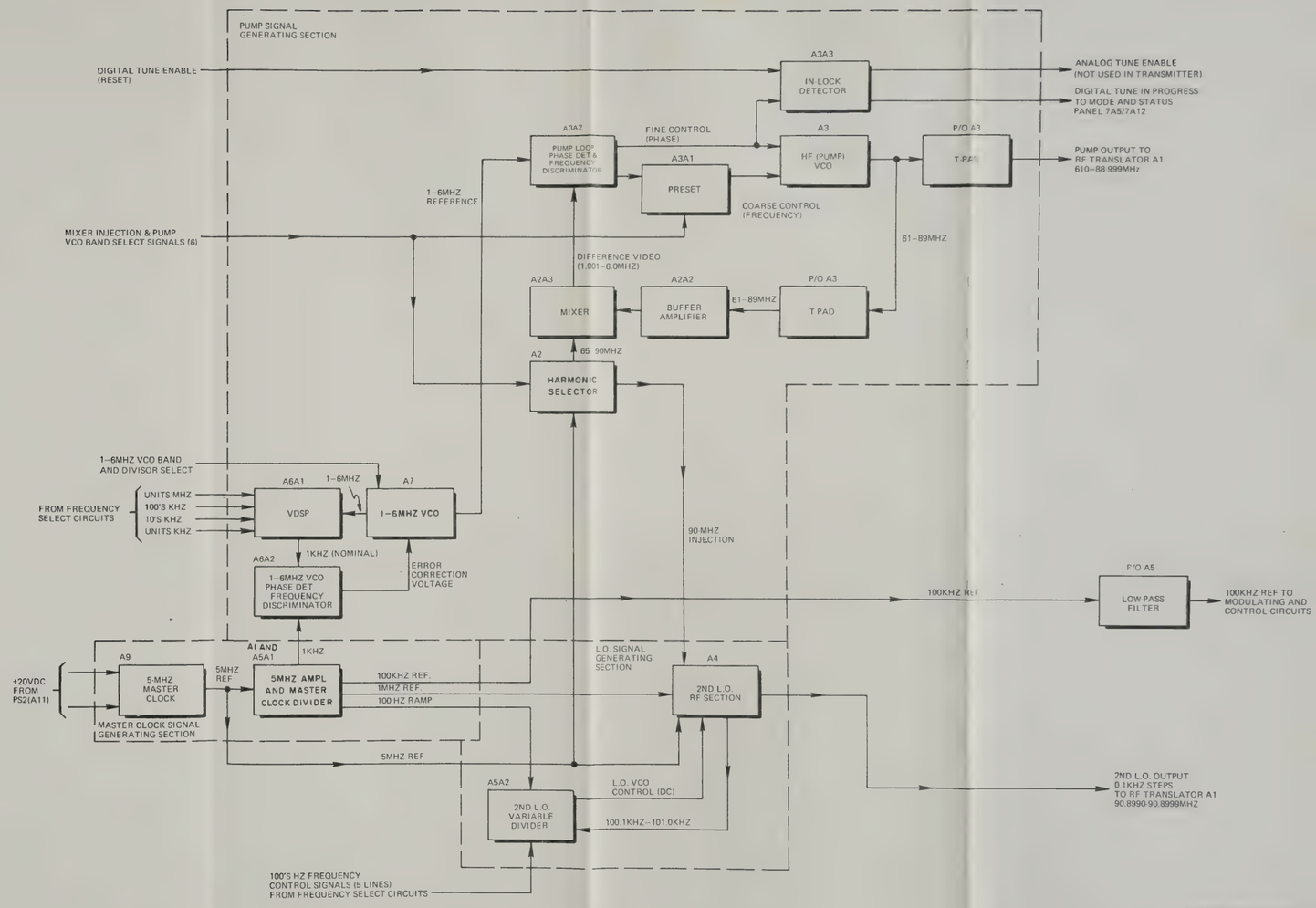


Figure FO–20. Frequency synthesizer A2, detailed block diagram.

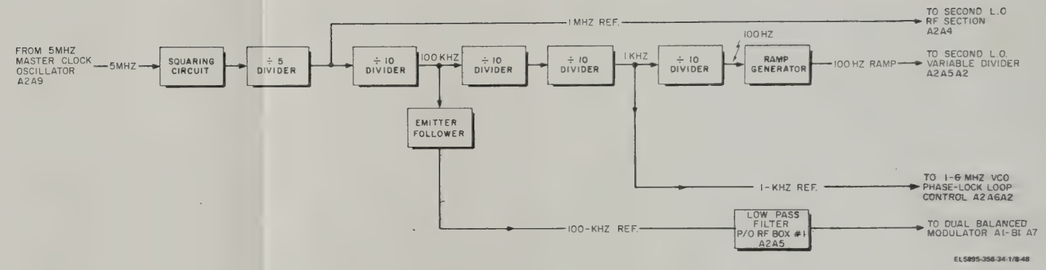
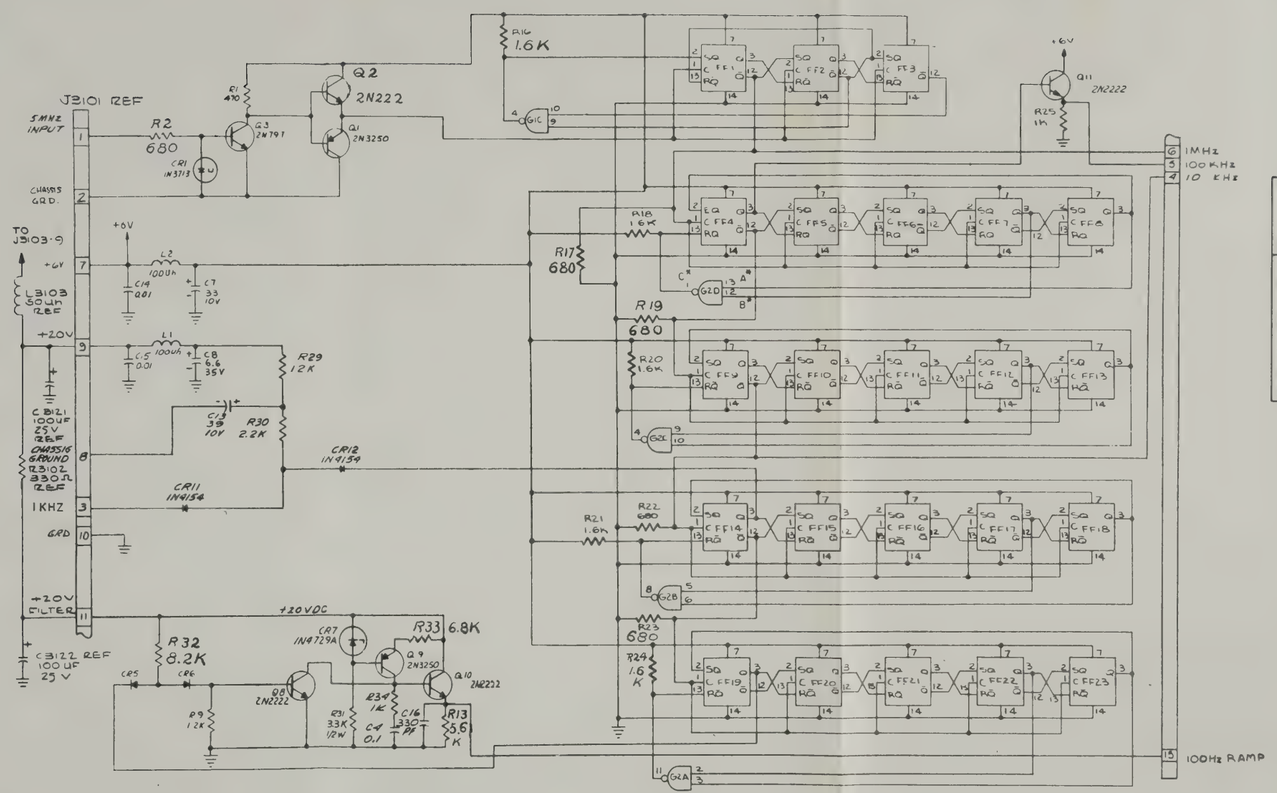
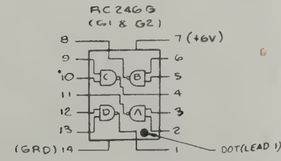


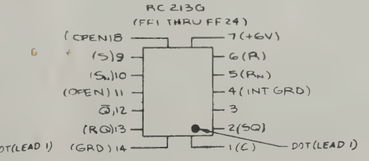
Figure FO–21. Master clock divider A2A5A1, block diagram.



RC 2469 (G1 & G2)



RC 2130 (FF1 THRU FF24)



SQ	RQ	Q(n+1)
0	1	1
1	0	0
1	1	Qn

LOGIC DEFINITION:
1 - STATE ~ 2V
0 - STATE ~ 0.3V

STATE	FF1 SQ	FF1 RQ	FF1 Qn	FF1 Qn+1	FF2 SQ	FF2 RQ	FF2 Qn	FF2 Qn+1	FF3 SQ	FF3 RQ	FF3 Qn	FF3 Qn+1	G1-C 9	G1-C 10	G1-C 4
0	0	1	0	1	0	1	0	1	0	1	0	1	1	1	0
1	0	1	1	0	1	0	1	0	1	0	1	0	1	1	1
2	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1
3	1	0	0	1	1	0	1	0	0	1	1	0	0	0	1
4	1	1	0	1	1	0	0	1	1	0	1	0	1	0	1

STATE	FF19 FF14 FF9 FF4 SQ	RQ	Qn	Qn+1	FF20 FF15 FF10 FF5 SQ	RQ	Qn	Qn+1	FF21 FF16 FF11 FF6 SQ	RQ	Qn	Qn+1	FF22 FF17 FF12 FF7 SQ	RQ	Qn	Qn+1	FF23 FF18 FF13 FF8 SQ	RQ	Qn	Qn+1	G2A G2B G2C G2D A*	B*	C*
0	0	1	0	1	0	1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	0	1
1	0	1	1	0	0	1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	0	1
2	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	1
3	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	1
4	0	1	1	0	0	1	1	0	0	1	0	1	1	0	1	0	1	0	0	0	0	0	1
5	1	0	1	0	0	1	1	0	0	1	0	1	1	0	1	0	1	0	0	0	0	0	1
6	1	0	0	1	0	1	1	0	0	1	0	1	1	0	1	0	1	0	0	0	0	0	1
7	1	0	0	1	1	0	0	1	0	1	1	0	1	0	1	0	1	0	0	0	0	0	1
8	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0	0	0	0	0	1
9	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0	0	0	0	0	1

*G2D A = PIN 13, B = PIN 12, C = PIN 1
G2C A = 9, B = 10, C = 4
G2B A = 5, B = 6, C = 8
G2A A = 2, B = 3, C = 11

NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A5A1
   SECONDARY TRANSMITTER 6A11A2A5A1
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS.
4. ALL DIODES ARE 1N4154.

EL5895-356-34-1/8-49

Figure FO–22. Master clock divider A2A5A1, schematic diagram.

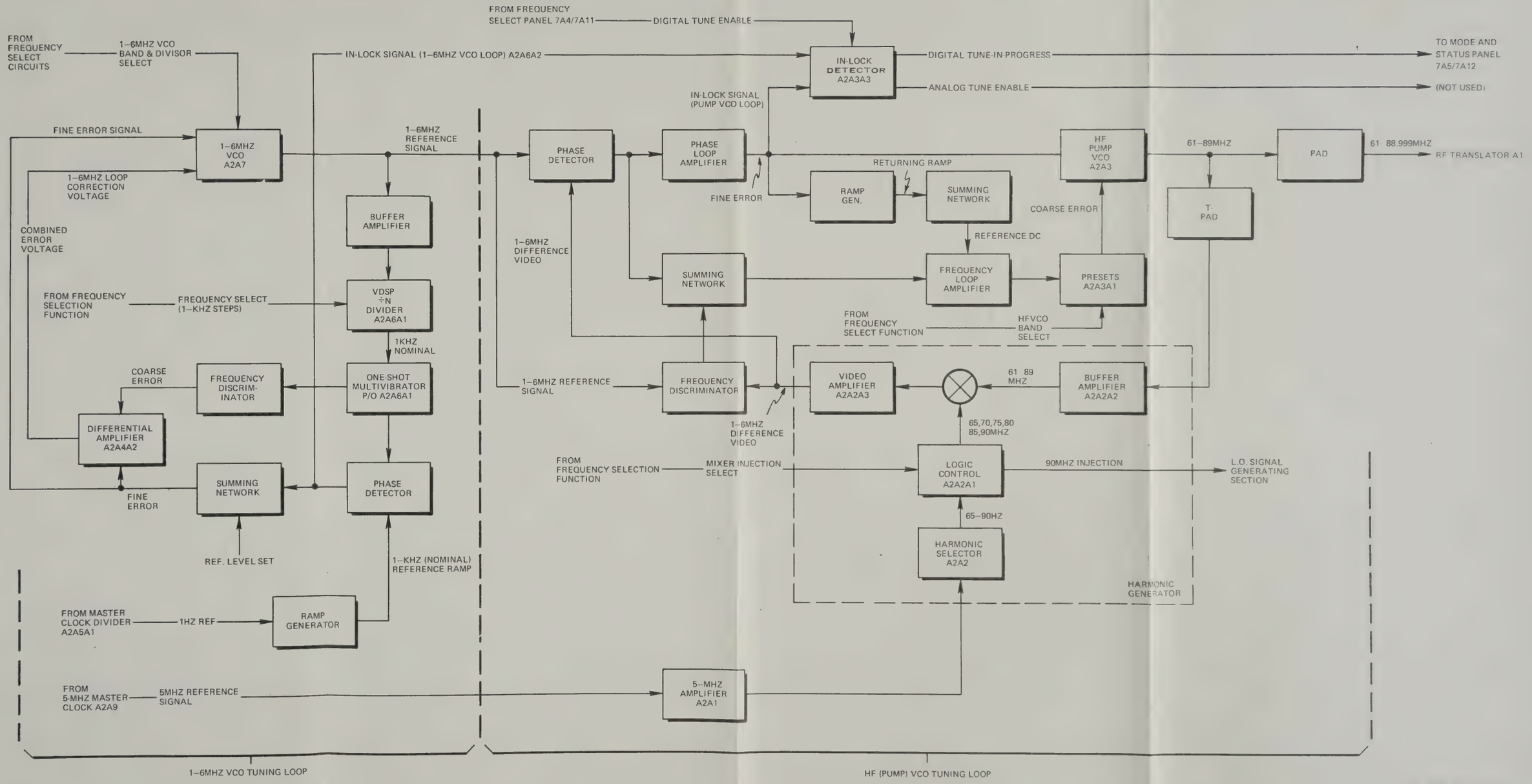
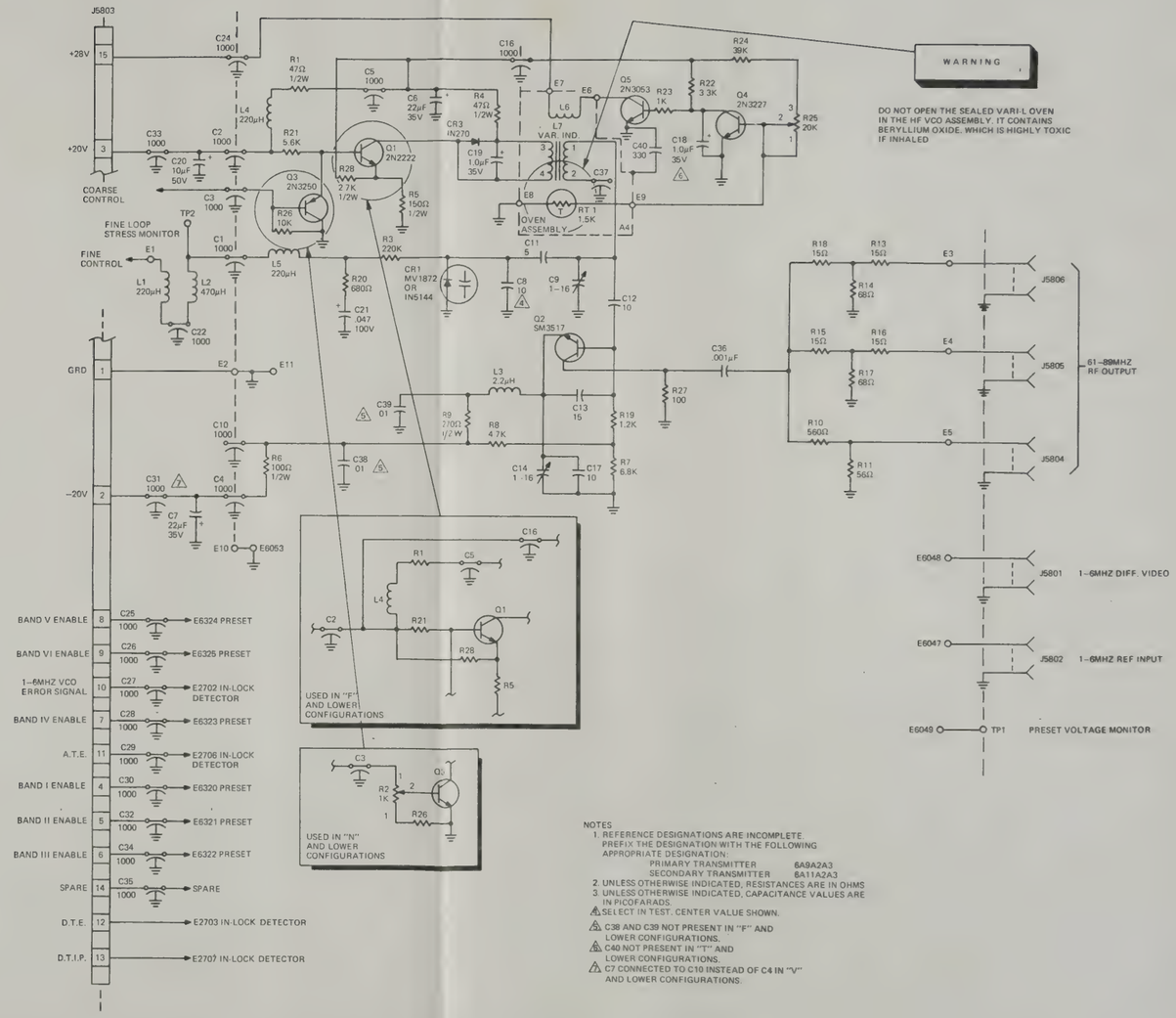
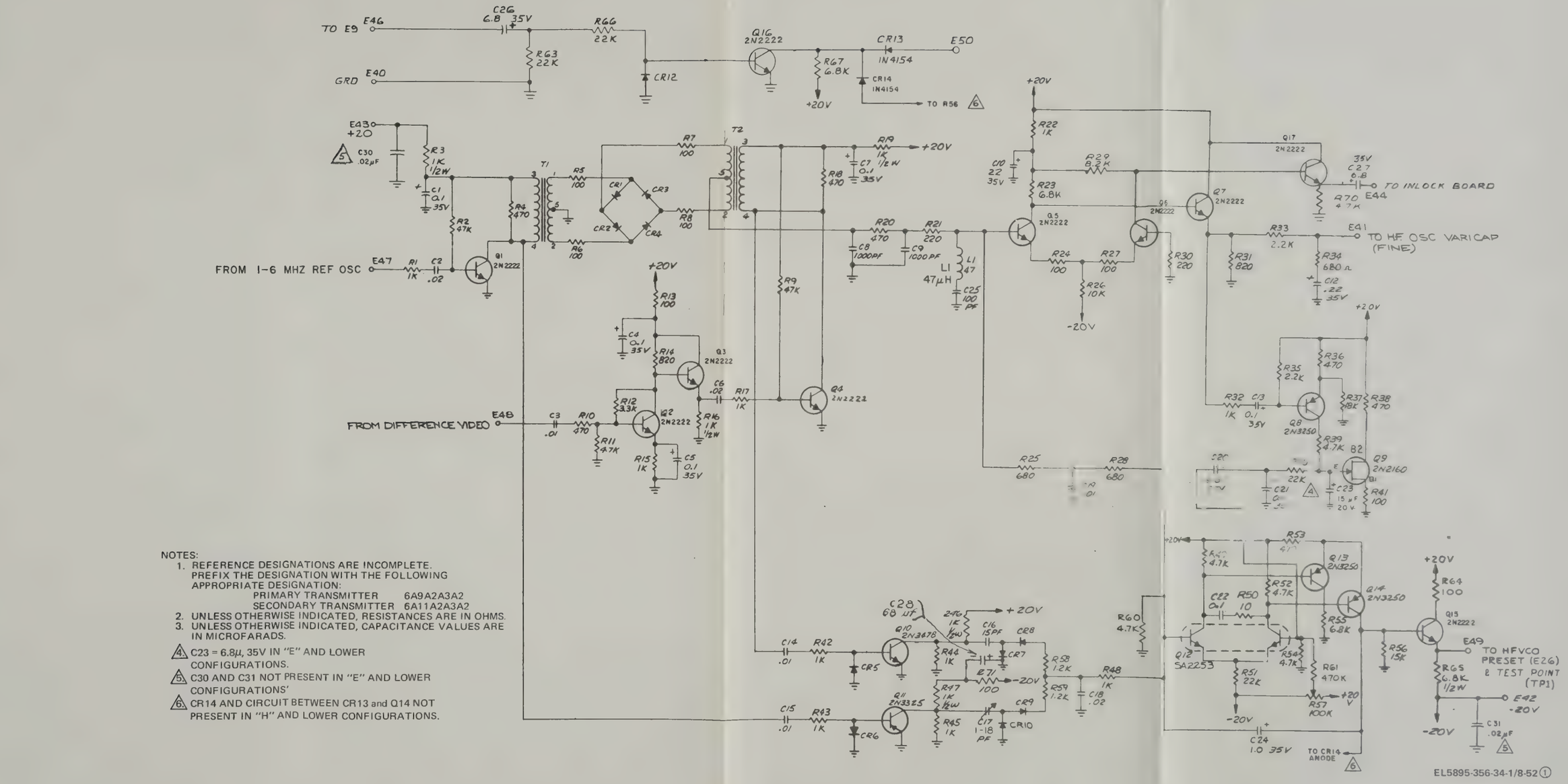


Figure FO–23. Hf (pump) VCO and 1–6-MHz VCO tuning loops, block diagram.



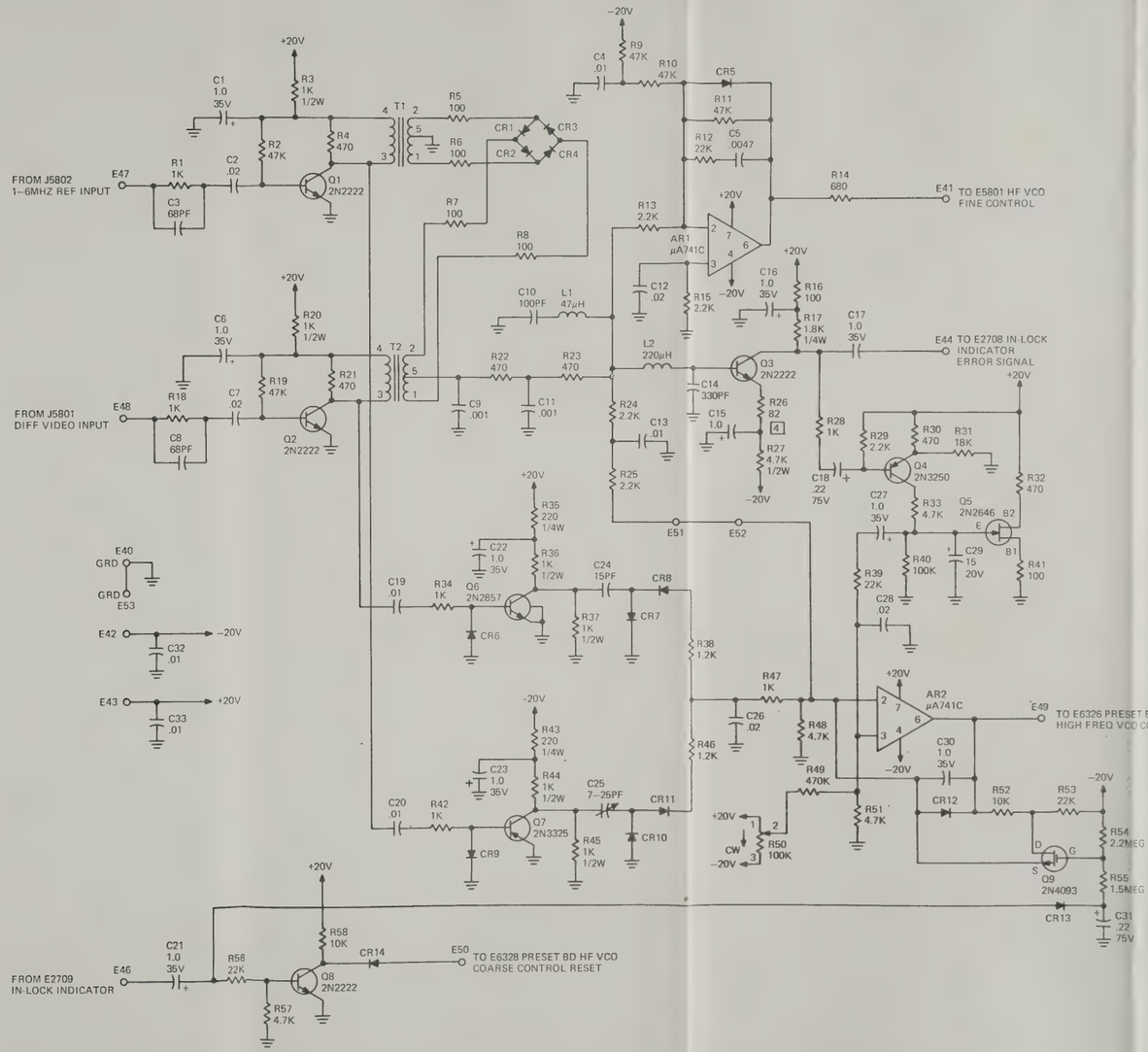
NOTES
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A3
   SECONDARY TRANSMITTER 6A11A2A3
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN PICOFARADS.
4. SELECT IN TEST. CENTER VALUE SHOWN.
5. C38 AND C39 NOT PRESENT IN "F" AND LOWER CONFIGURATIONS.
6. C40 NOT PRESENT IN "T" AND LOWER CONFIGURATIONS.
7. C7 CONNECTED TO C10 INSTEAD OF C4 IN "V" AND LOWER CONFIGURATIONS.

Figure FO–24. Hf VCO A2A3, schematic diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A3A2
   SECONDARY TRANSMITTER 6A11A2A3A2
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS.
4. C23 = 6.8μ, 35V IN "E" AND LOWER CONFIGURATIONS.
5. C30 AND C31 NOT PRESENT IN "E" AND LOWER CONFIGURATIONS'
6. CR14 AND CIRCUIT BETWEEN CR13 and Q14 NOT PRESENT IN "H" AND LOWER CONFIGURATIONS.

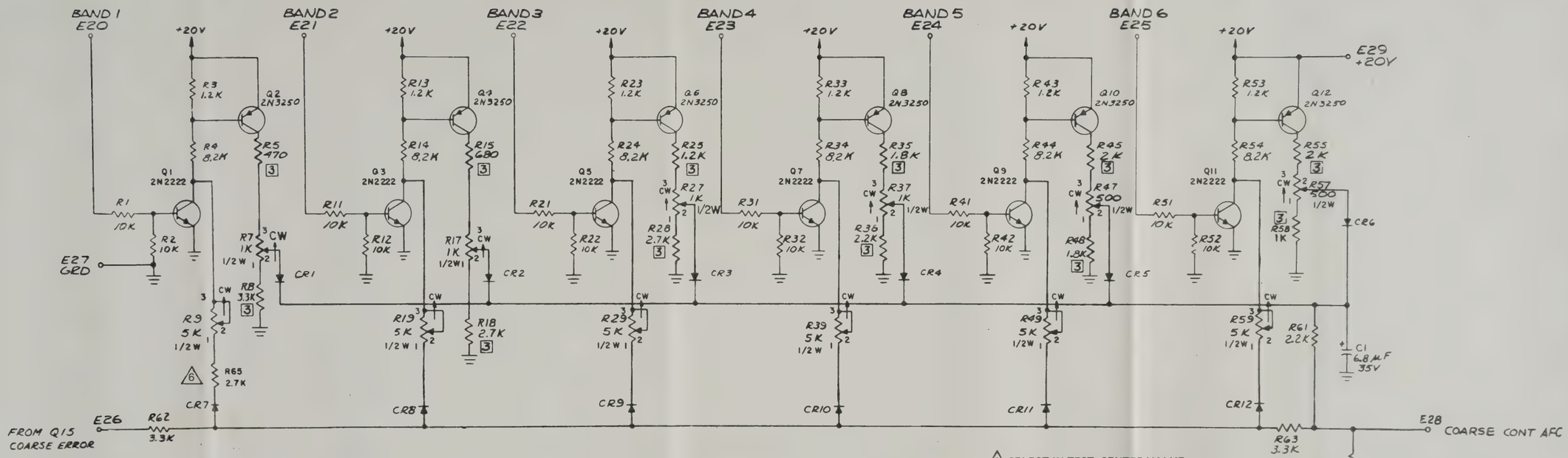
Figure FO–25①. Control loop A2A3A2 (233–00–274), schematic diagram (sheet 1 of 2).



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A3A2
   SECONDARY TRANSMITTER 6A11A2A3A2
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS.
4. SELECT IN TEST, CENTER VALUE SHOWN.
5. UNLESS OTHERWISE INDICATED ALL DIODES ARE IN4154.

EL5895-356-34-1/8-52 ②

Figure FO-25②. Control loop A2A3A2 (233-00-640), schematic diagram (sheet 2 of 2).



NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A3A1
   SECONDARY TRANSMITTER 6A11A2A3A1
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.

△3 SELECT IN TEST, CENTER VALUE SHOWN.

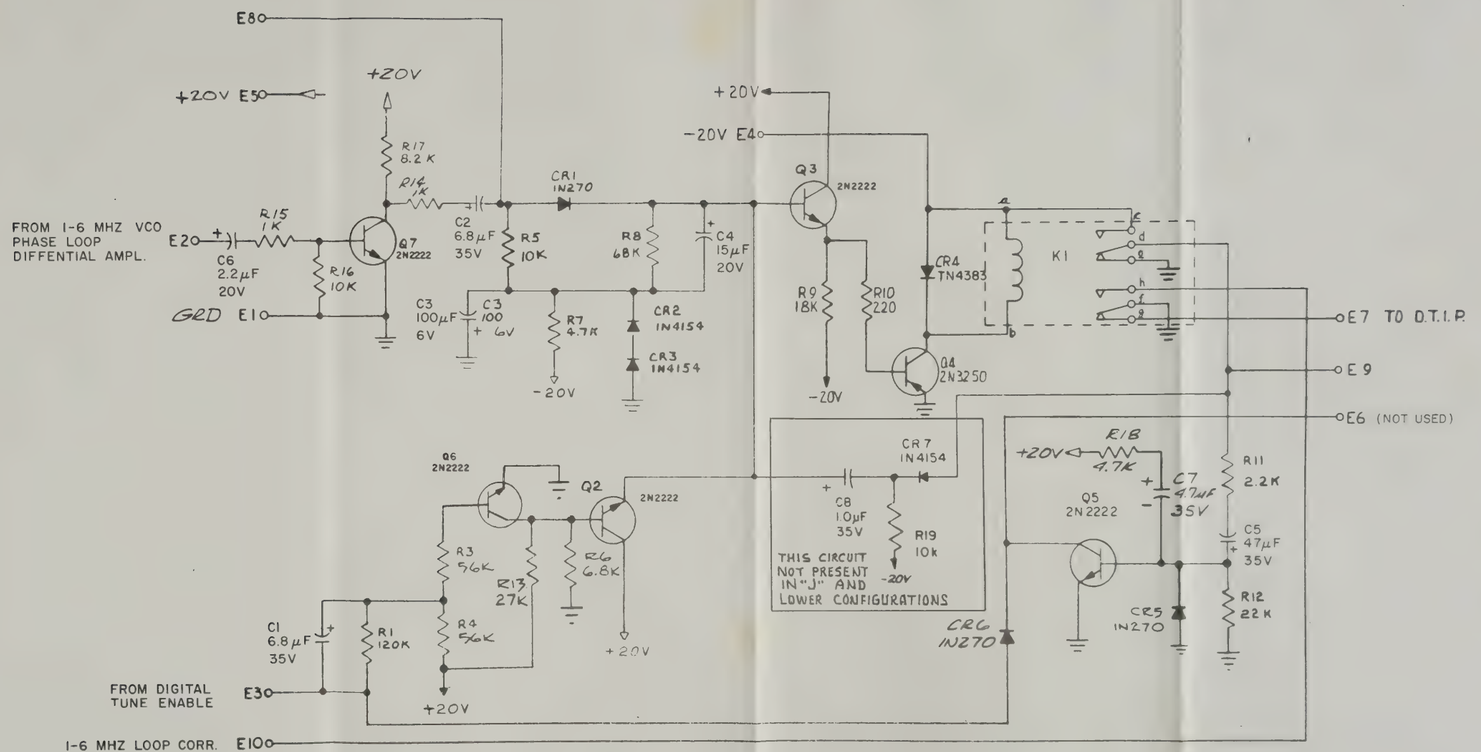
4. UNLESS OTHERWISE INDICATED, DIODES ARE IN < ARE IN 4154.

△5 R64 is 2.2K AND NOT S.I.T. IN "G" AND LOWER CONFIGURATIONS.

△6 R65 NOT PRESENT IN "M" AND LOWER CONFIGURATIONS.

EL5895-356-34-1/8-53

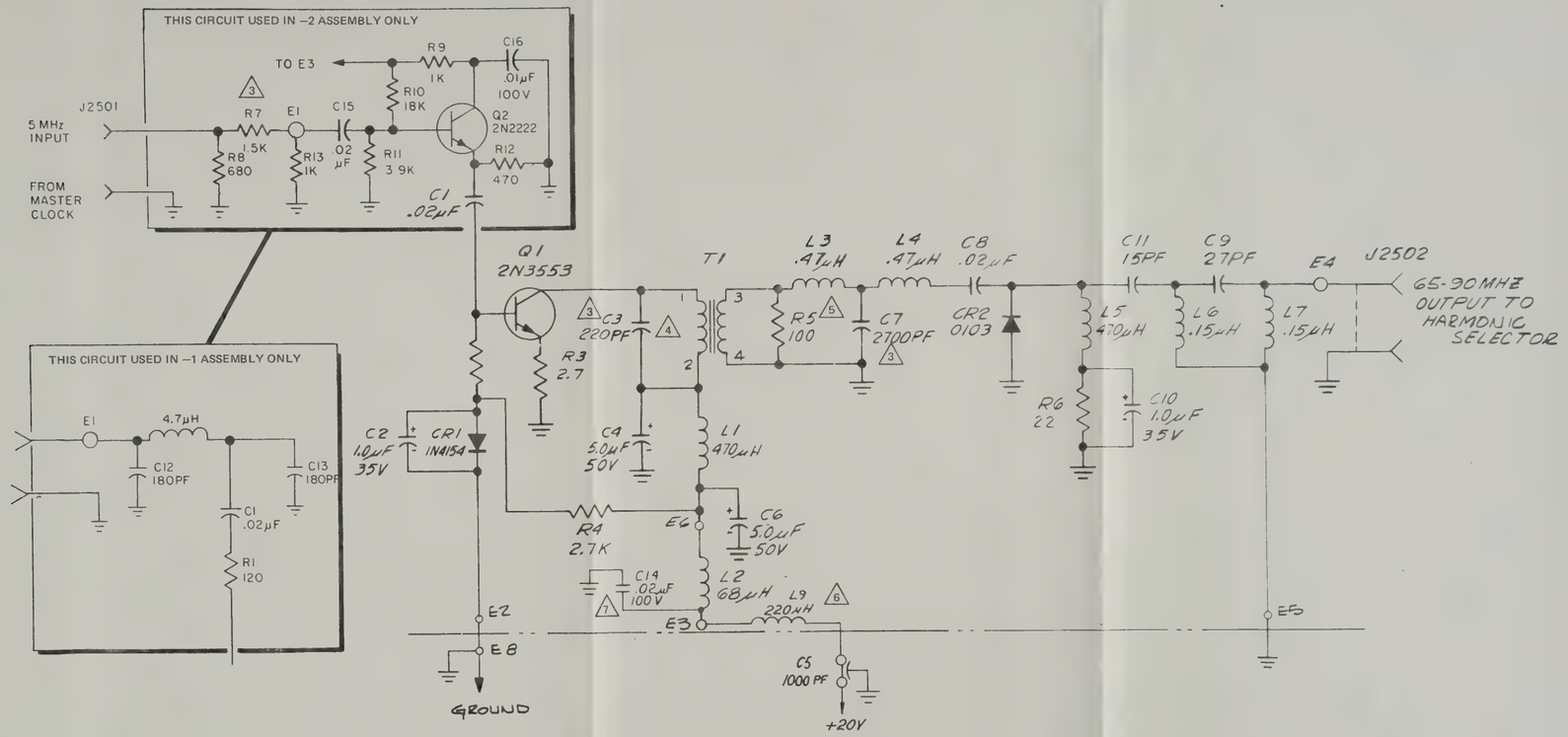
Figure FO-26. Preset A2A3A1, schematic diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A3A3
   SECONDARY TRANSMITTER 6A11A2A3A3
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.

EL5895-356-34-1/8-54

Figure FO-27. In-lock detector A2A3A3, schematic diagram.



NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A1
   SECONDARY TRANSMITTER 6A11A2A1

△2 UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
△3 SELECT IN TEST, CENTER VALUE SHOWN.
△4 C3 IS NOT SELECT IN TEST IN "L" AND LOWER CONFIGURATION OF THIS ASSY.
△5 R5 IS NOT SELECT IN TEST IN "C" AND LOWER CONFIGURATIONS OF THE 1 & 2 ASSYS.
△6 L9 NOT PRESENT IN –1 ASSEMBLY (E3 IS CONNECTED DIRECTLY TO C5).
△7 C14 NOT PRESENT IN –1 ASSEMBLY USING TYPE 233-00-595-1 COMPONENT BOARD.

EL5895-356-34-1/8-55

Figure FO–28. 5-MHz amplifier A2A1, schematic diagram.

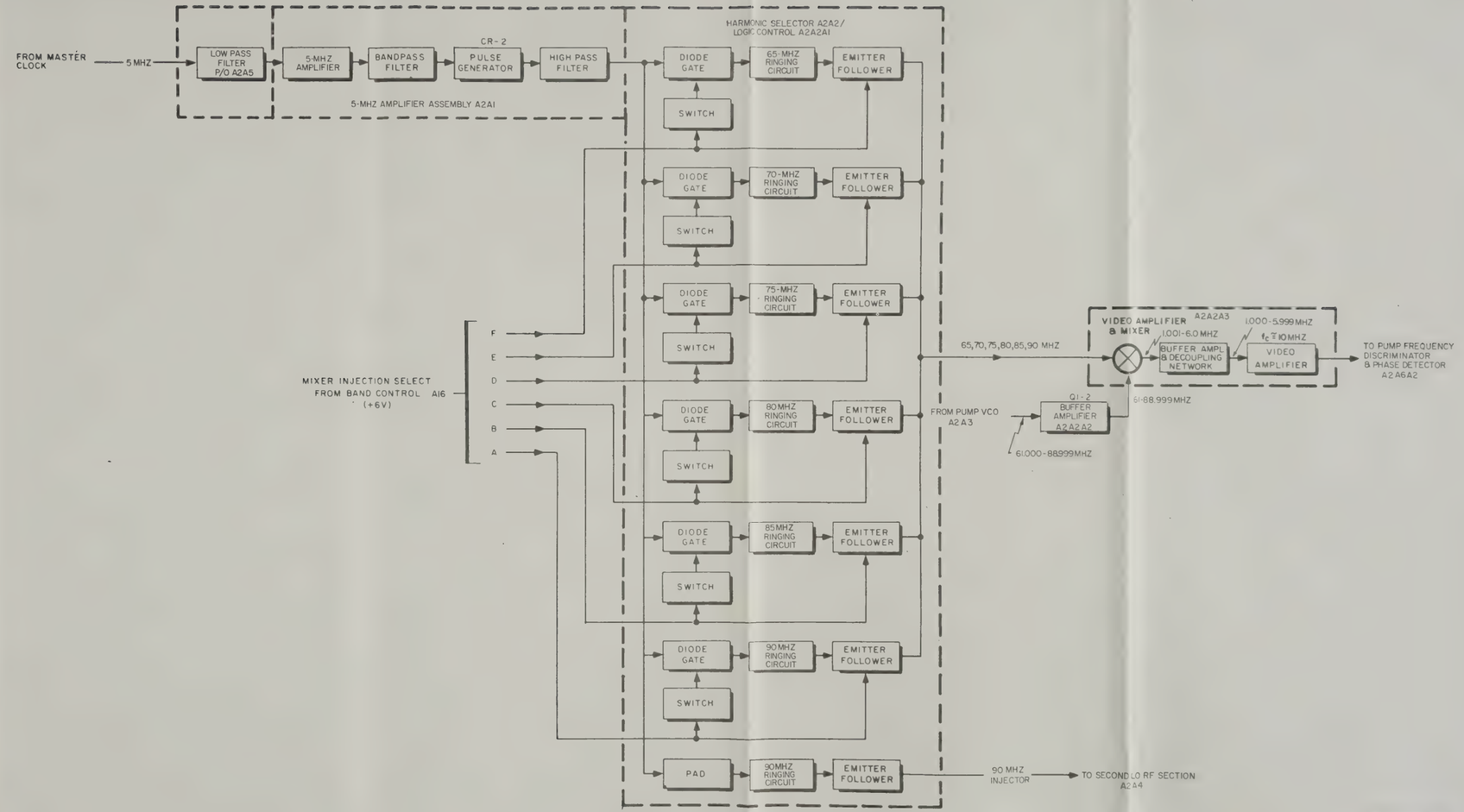
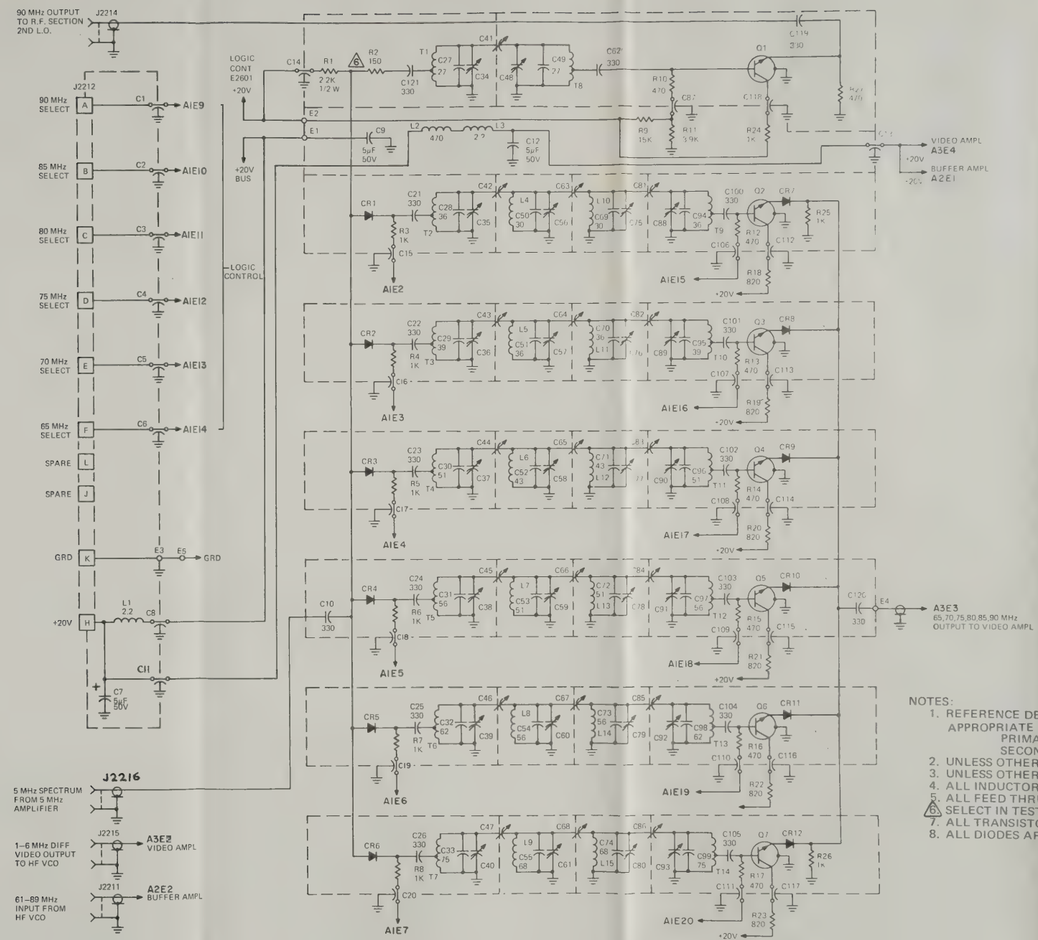


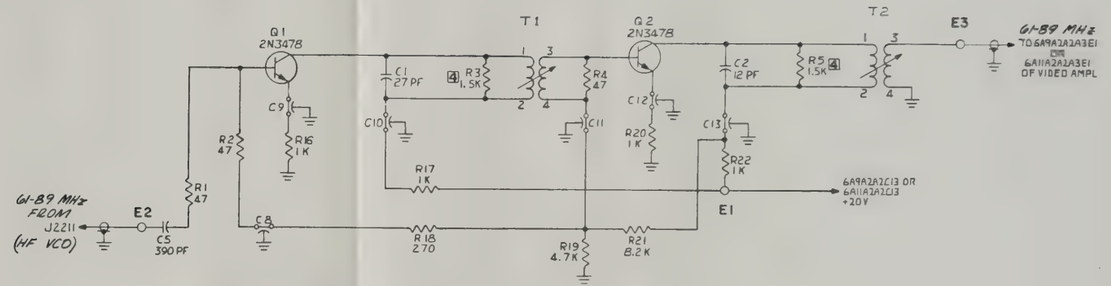
Figure FO–29. Harmonic generator and mixer, block diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE, PREFIX WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A2
   SECONDARY TRANSMITTER 6A11A2A2
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN PICOFARADS.
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. ALL FEED THRU CAPACITORS ARE 1000 PICOFARADS.
6. (S) SELECT IN TEST, CENTER VALUE SHOWN.
7. ALL TRANSISTORS ARE 2N918.
8. ALL DIODES ARE 1N270.

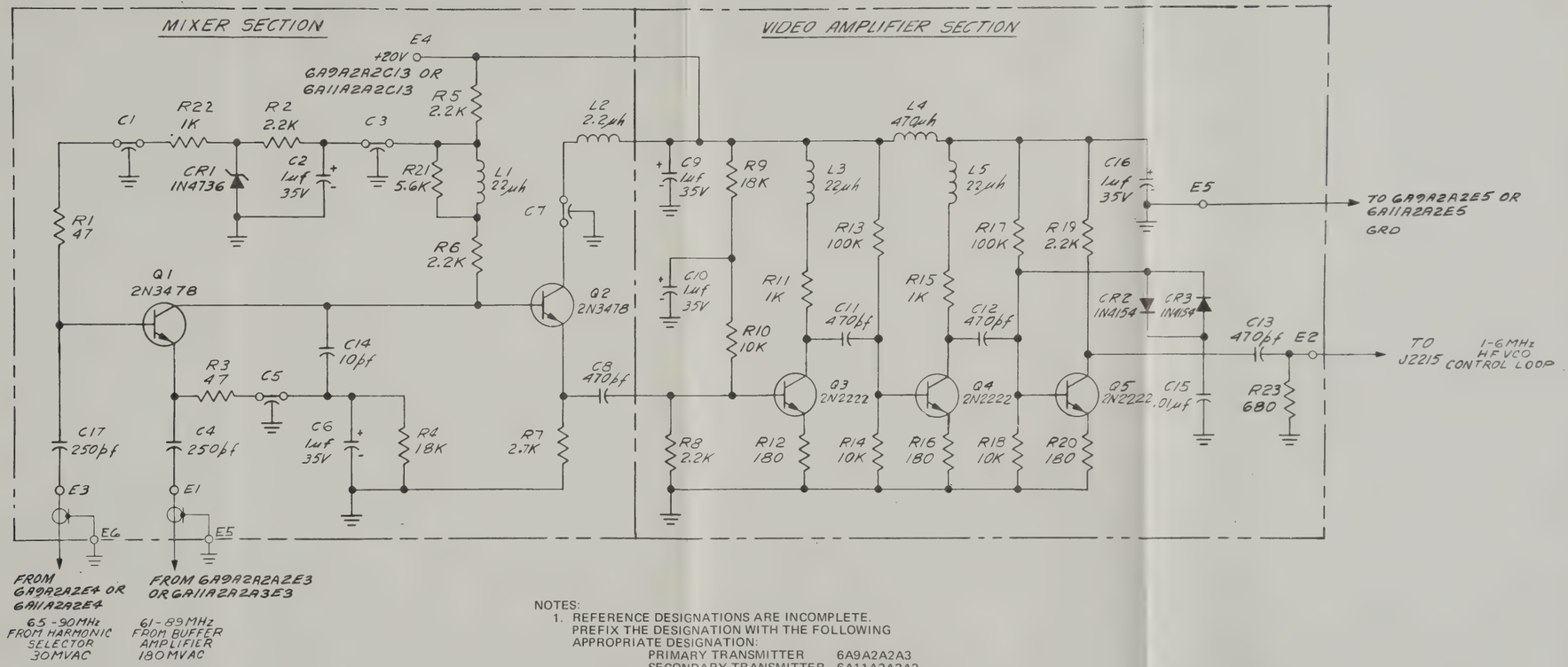
EL5895–356–34–1/8–57

Figure FO–30. Harmonic selector A2A2, schematic diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A2A2
   SECONDARY TRANSMITTER 6A11A2A2A2
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.
4. SELECT IN TEST, CENTER VALUE SHOWN.

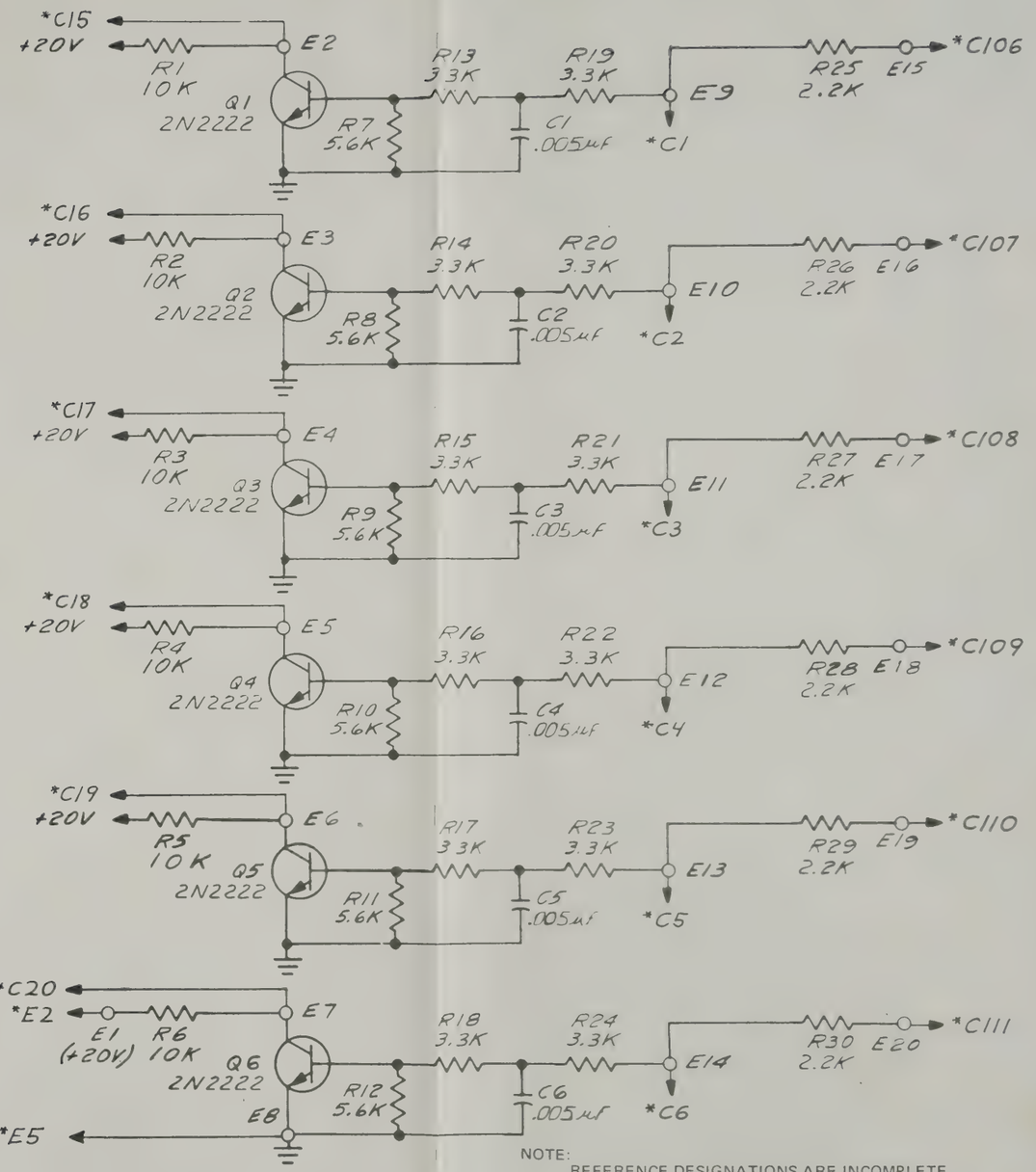
Figure FO–31. Buffer amplifier A2A2A2, schematic diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE.
   PREFIX THE DESIGNATION WITH THE FOLLOWING
   APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A2A3
   SECONDARY TRANSMITTER 6A11A2A2A3
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.

EL5895-356-34-1/8-59

Figure FO–32. Video amplifier and mixer A2A2A3, schematic diagram.



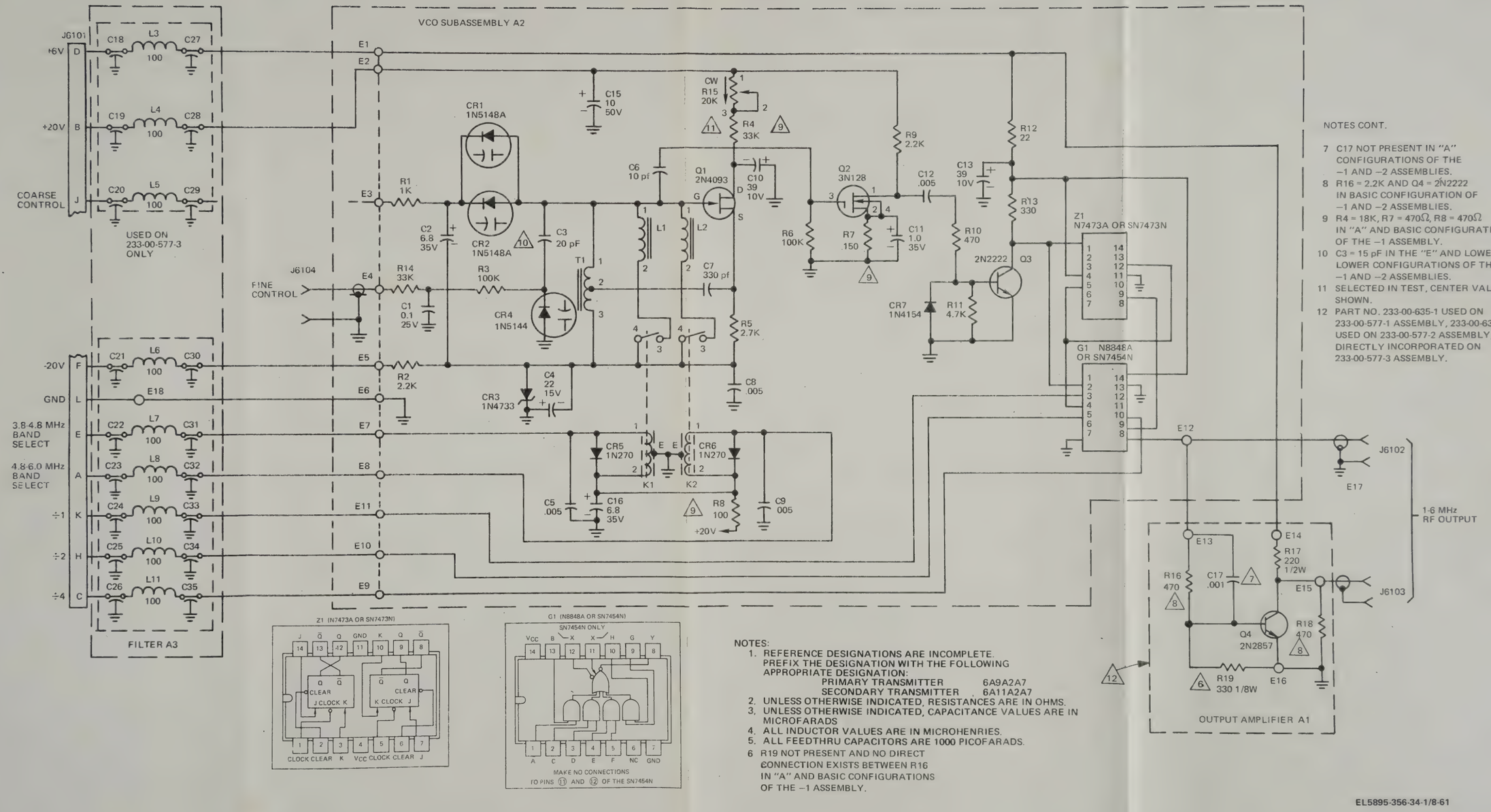
NOTE:
REFERENCE DESIGNATIONS ARE INCOMPLETE.
PREFIX THE DESIGNATION WITH THE FOLLOWING
APPROPRIATE DESIGNATION:

PRIMARY TRANSMITTER	6A9A2A2A1
SECONDARY TRANSMITTER	6A11A2A2A1

*PREFIX THESE COMPONENTS WITH
6A9A2A2 OR 6A11A2A2 AS REQUIRED.

EL5895-356-34-1/8-60

Figure FO–33. Logic control A2A2A1, schematic diagram.



NOTES:

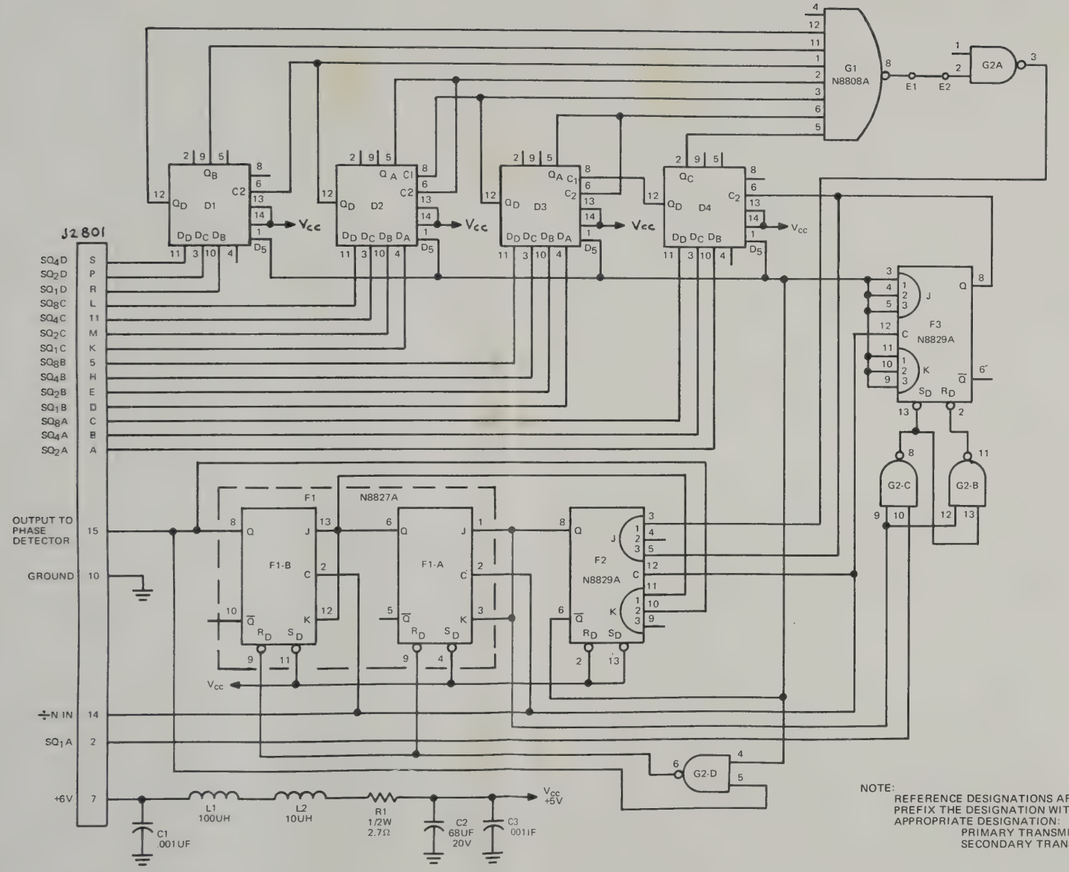
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A7
   SECONDARY TRANSMITTER 6A11A2A7
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.
6. R19 NOT PRESENT AND NO DIRECT CONNECTION EXISTS BETWEEN R16 IN "A" AND BASIC CONFIGURATIONS OF THE –1 ASSEMBLY.

NOTES CONT.

7. C17 NOT PRESENT IN "A" CONFIGURATIONS OF THE –1 AND –2 ASSEMBLIES.
8. R16 = 2.2K AND Q4 = 2N2222 IN BASIC CONFIGURATION OF –1 AND –2 ASSEMBLIES.
9. R4 = 18K, R7 = 470Ω, R8 = 470Ω IN "A" AND BASIC CONFIGURATIONS OF THE –1 ASSEMBLY.
10. C3 = 15 pF IN THE "E" AND LOWER LOWER CONFIGURATIONS OF THE –1 AND –2 ASSEMBLIES.
11. SELECTED IN TEST, CENTER VALUE SHOWN.
12. PART NO. 233-00-635-1 USED ON 233-00-577-1 ASSEMBLY, 233-00-638-2 USED ON 233-00-577-2 ASSEMBLY, DIRECTLY INCORPORATED ON 233-00-577-3 ASSEMBLY.

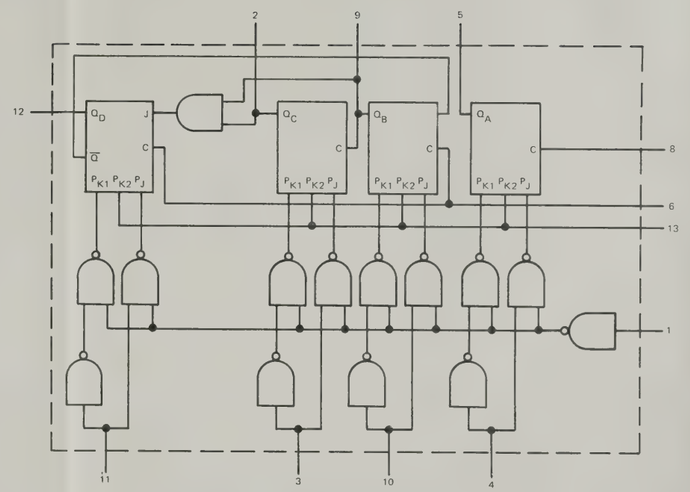
EL5895-356-34-1/8-61

Figure FO–34. 1–6-MHz VCO A2A7, schematic diagram.

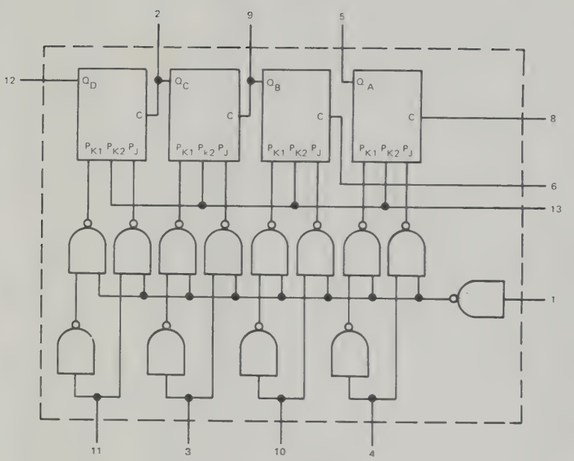


NOTE:
REFERENCE DESIGNATIONS ARE INCOMPLETE.
PREFIX THE DESIGNATION WITH THE FOLLOWING
APPROPRIATE DESIGNATION:
PRIMARY TRANSMITTER 6A9A2A6A1
SECONDARY TRANSMITTER 6A11A2A6A1

N8280A
D2,D3,D4



N8281A
D1



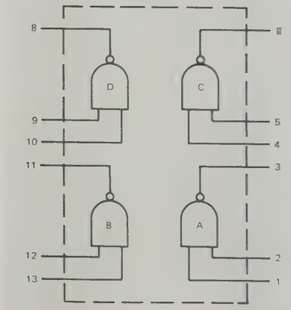
1's MHz DIGIT	*INPUTS S	P	R
0	0	0	1
1	0	0	0
2	1	0	0
3	0	1	1
4	0	1	0
5	0	0	1
6	0	1	0
7	0	0	0
8	0	1	1
9	0	1	0

DIGIT 100's KHz	10's KHz	1's KHz	*INPUTS L	11	M	K
	5	H	E	D		
	C	B	A	2		
0	1	0	0	1		
1	1	0	0	0		
2	0	1	1	1		
3	0	1	1	0		
4	0	1	0	1		
5	0	1	0	0		
6	0	0	1	1		
7	0	0	1	0		
8	0	0	0	1		
9	0	0	0	0		

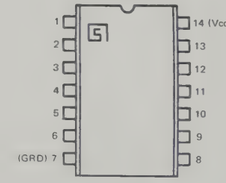
F2	F1 A	F1 B
0	0	0
·	·	·
·	0	0
1	1	0
1	0	1
1	1	1
0	0	0

CONTROL COUNT SEQUENCE

N8480A
G2



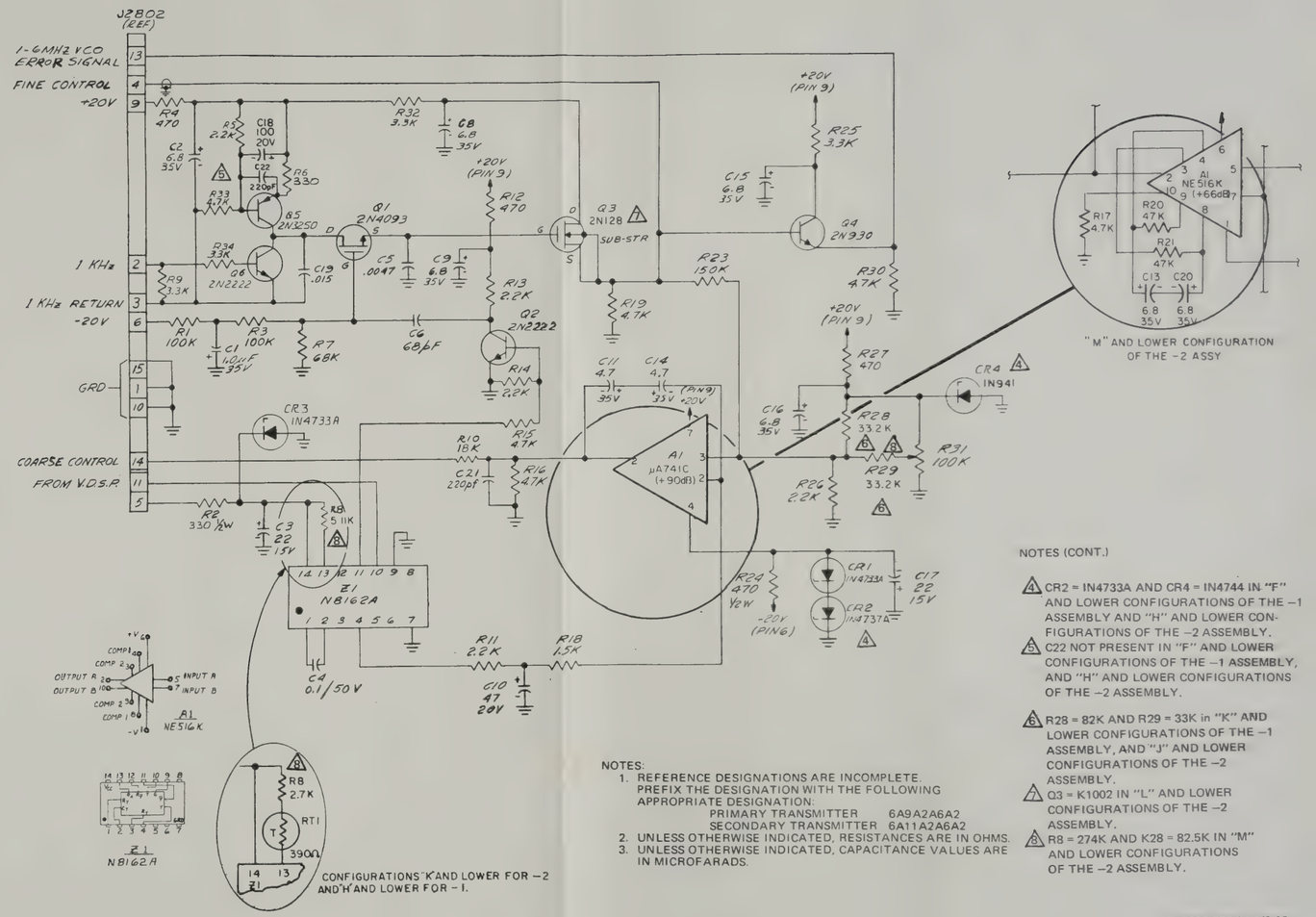
*1 = 4 VDC TYP.
0 = 0.25 VDC TYP.



I.C. PIN ORIENTATION

EL5895-356-34-1/8-62

Figure FO–35. Variable divider synthesizer pump (A2A6A1), schematic diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A6A2
   SECONDARY TRANSMITTER 6A11A2A6A2
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS.

NOTES (CONT.)

4. CR2 = IN4733A AND CR4 = IN4744 IN "F" AND LOWER CONFIGURATIONS OF THE –1 ASSEMBLY AND "H" AND LOWER CONFIGURATIONS OF THE –2 ASSEMBLY.
5. C22 NOT PRESENT IN "F" AND LOWER CONFIGURATIONS OF THE –1 ASSEMBLY, AND "H" AND LOWER CONFIGURATIONS OF THE –2 ASSEMBLY.
6. R28 = 82K AND R29 = 33K in "K" AND LOWER CONFIGURATIONS OF THE –1 ASSEMBLY, AND "J" AND LOWER CONFIGURATIONS OF THE –2 ASSEMBLY.
7. Q3 = K1002 IN "L" AND LOWER CONFIGURATIONS OF THE –2 ASSEMBLY.
8. R8 = 274K AND K28 = 82.5K IN "M" AND LOWER CONFIGURATIONS OF THE –2 ASSEMBLY.

EL5895-356-34-1/8-63

Figure FO–86. 1–6-MHz phase-lock loop A2A6A2, schematic diagram.

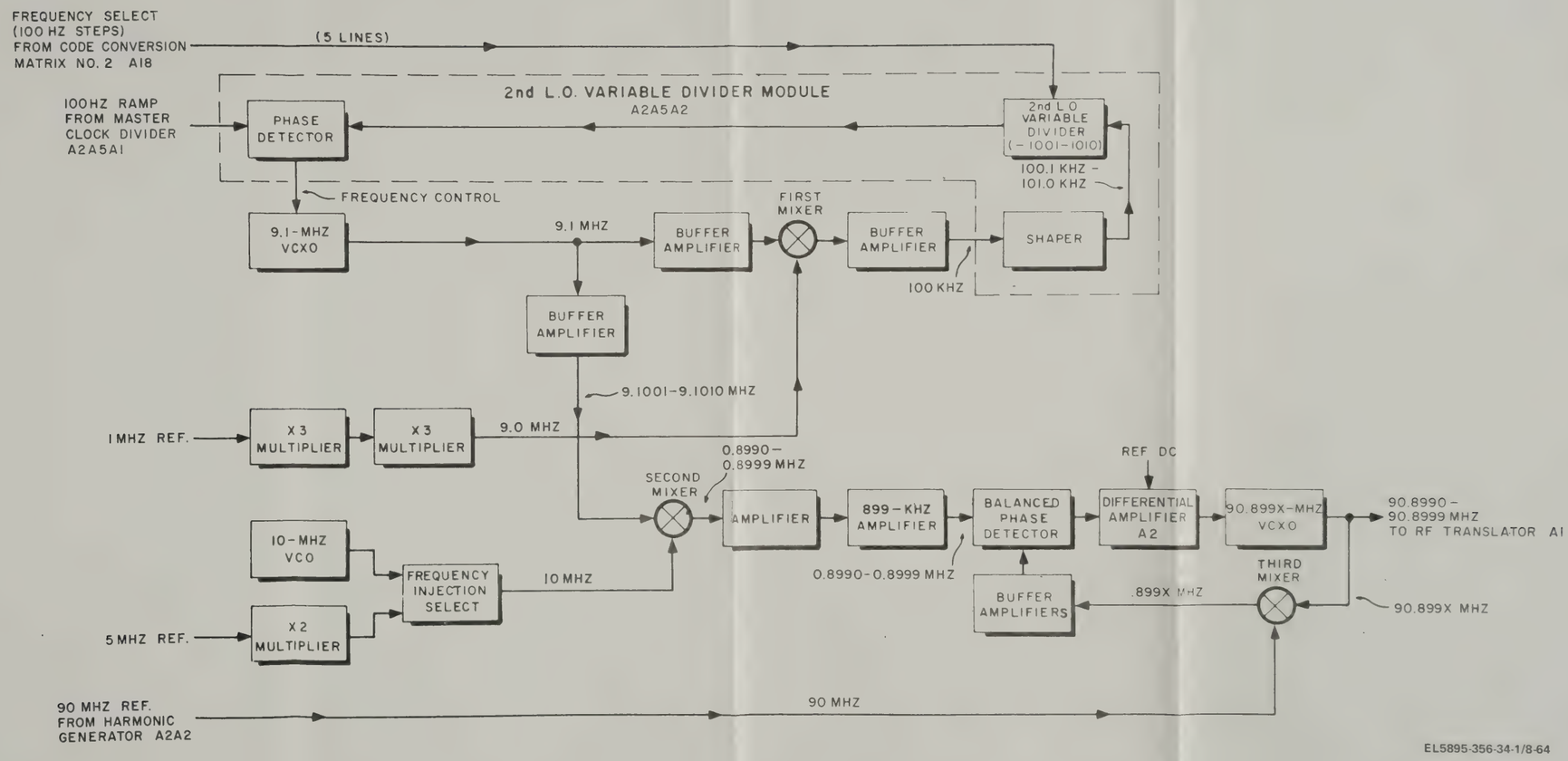
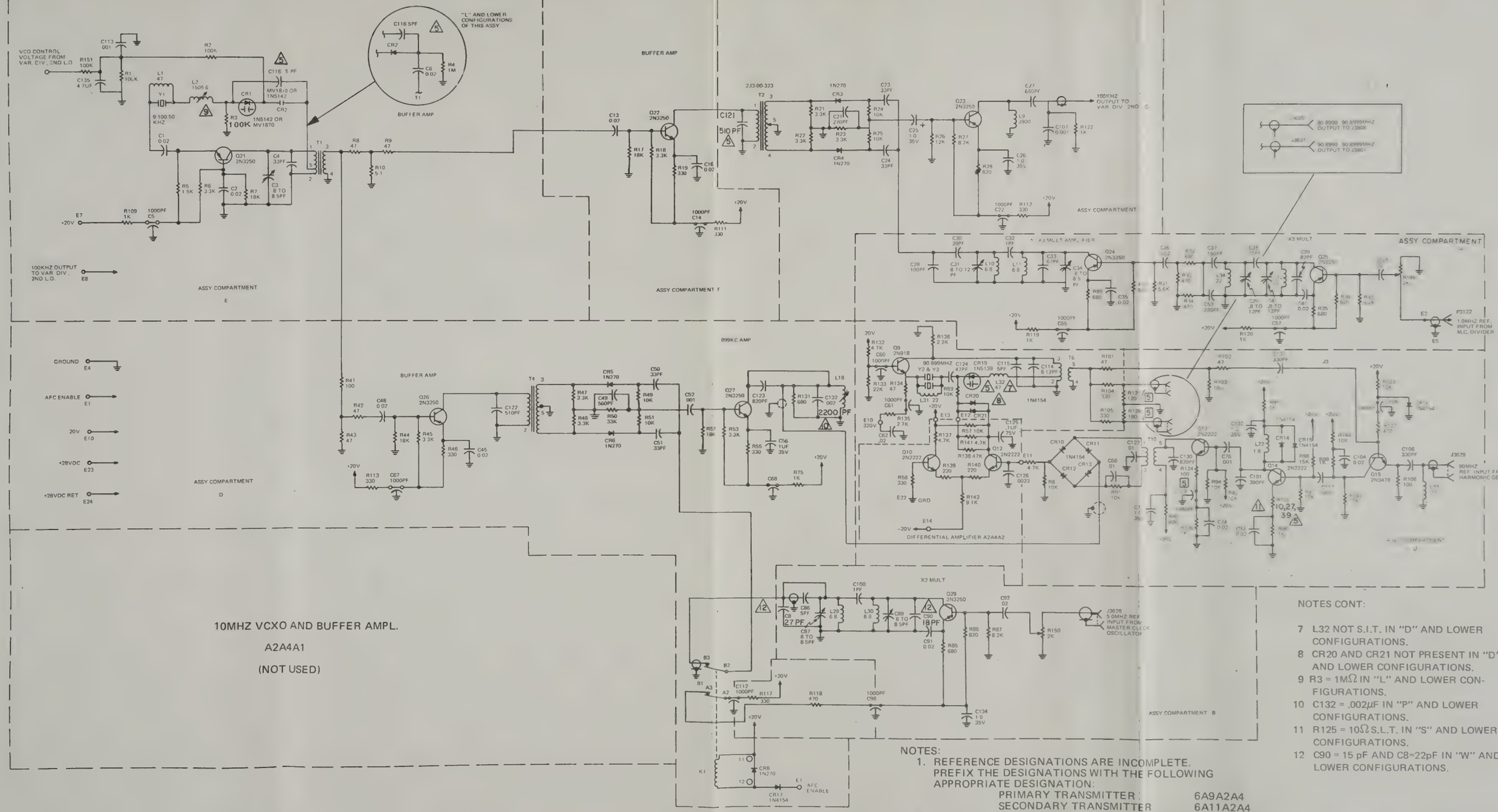


Figure FO-37. Second L.O. RF section A2A4 signal generating section, block diagram.



NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATIONS WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A4
   SECONDARY TRANSMITTER 6A11A2A4
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS.
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. SELECT IN TEST, CENTER VALUE SHOWN.
6. NO. 24 AWG STRANDED WIRE INSTEAD OF COAX CABLE IN "V" AND LOWER CONFIGURATIONS.

NOTES CONT:

7 L32 NOT S.I.T. IN "D" AND LOWER CONFIGURATIONS.
8 CR20 AND CR21 NOT PRESENT IN "D" AND LOWER CONFIGURATIONS.
9 R3 = 1MΩ IN "L" AND LOWER CONFIGURATIONS.
10 C132 = .002μF IN "P" AND LOWER CONFIGURATIONS.
11 R125 = 10Ω S.L.T. IN "S" AND LOWER CONFIGURATIONS.
12 C90 = 15 pF AND C8=22pF IN "W" AND LOWER CONFIGURATIONS.

EL5895-356-34-1/8-65

Figure FO–38. RF section 2nd L.O. A2A4, schematic diagram.

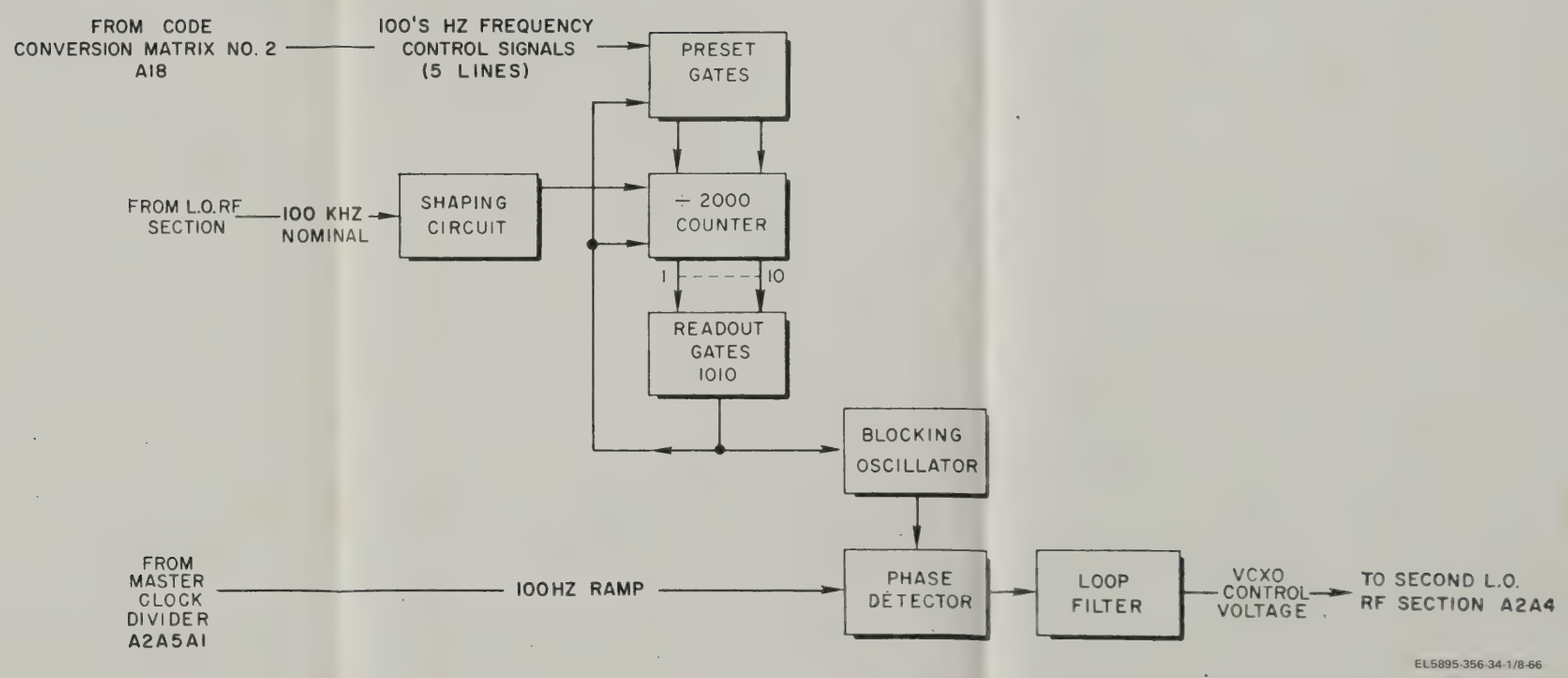
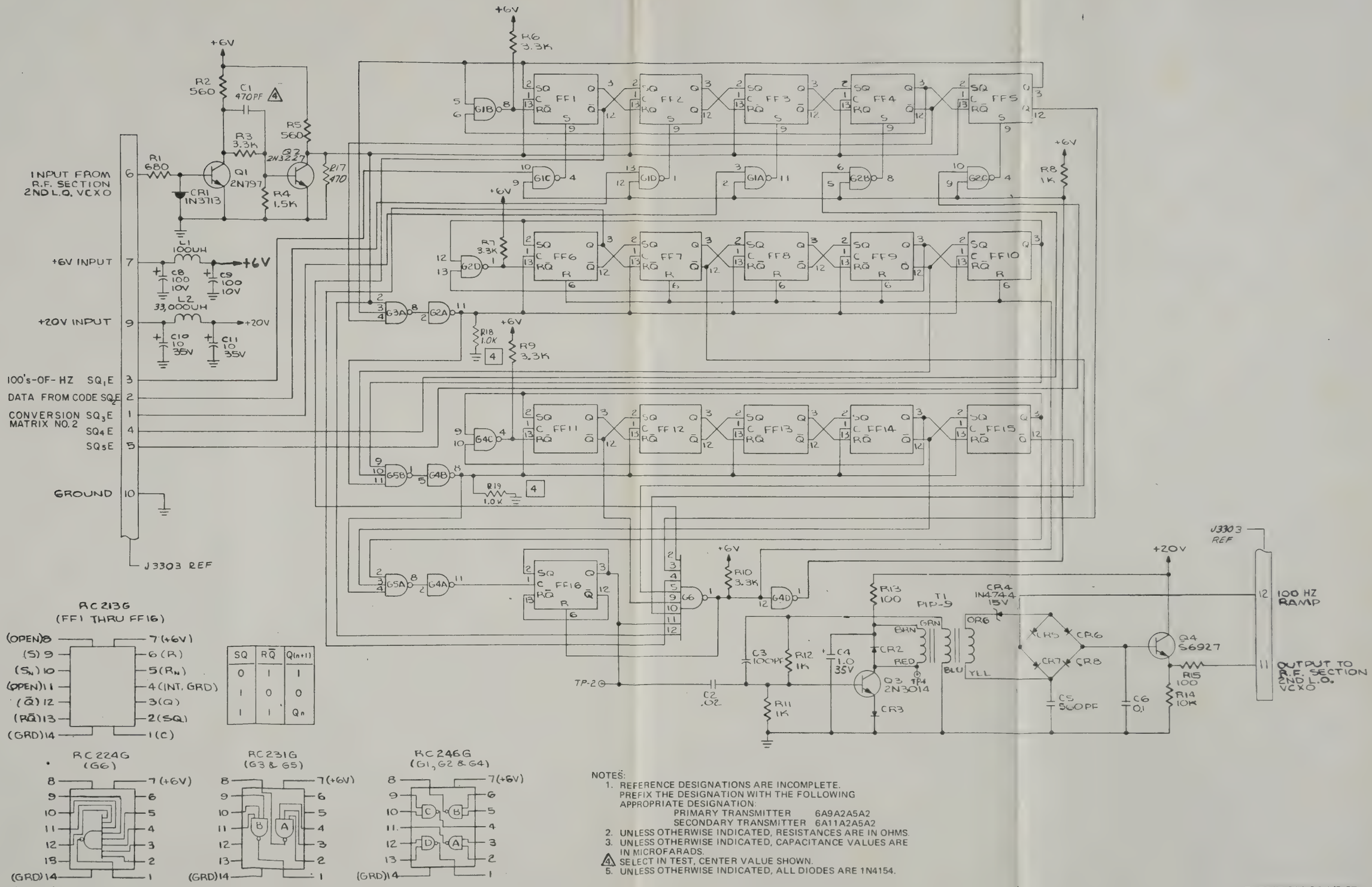


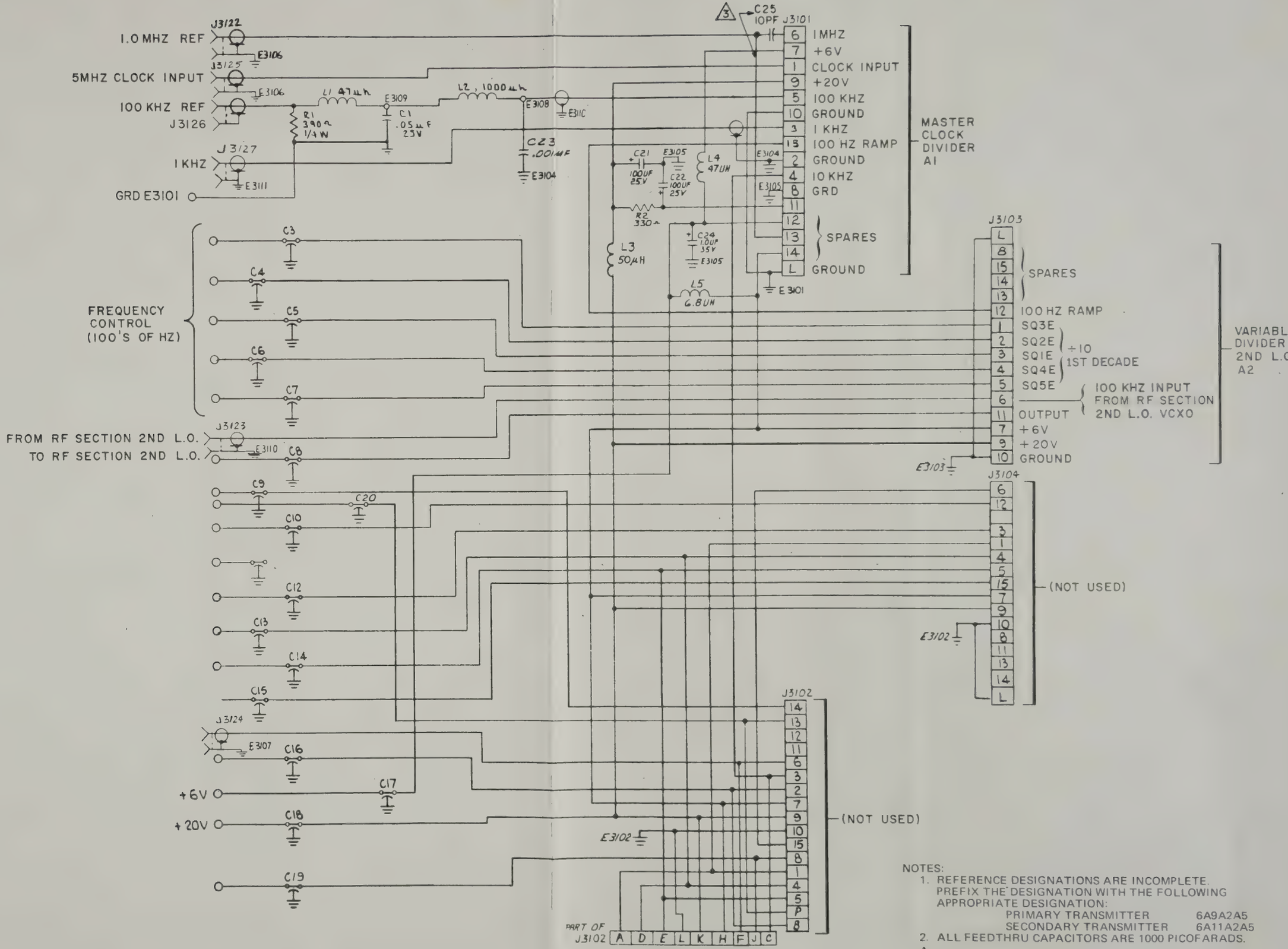
Figure FO–39. Variable divider 2nd L.O. A2A5A2, block diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A5A2
   SECONDARY TRANSMITTER 6A11A2A5A2
2. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS.
3. UNLESS OTHERWISE INDICATED, CAPACITANCE VALUES ARE IN MICROFARADS.
4. SELECT IN TEST, CENTER VALUE SHOWN.
5. UNLESS OTHERWISE INDICATED, ALL DIODES ARE 1N4154.

EL5895-356-34-1/8-67

Figure FO-40. Variable divider 2nd L.O. A2A5A2, schematic diagram.



NOTES:

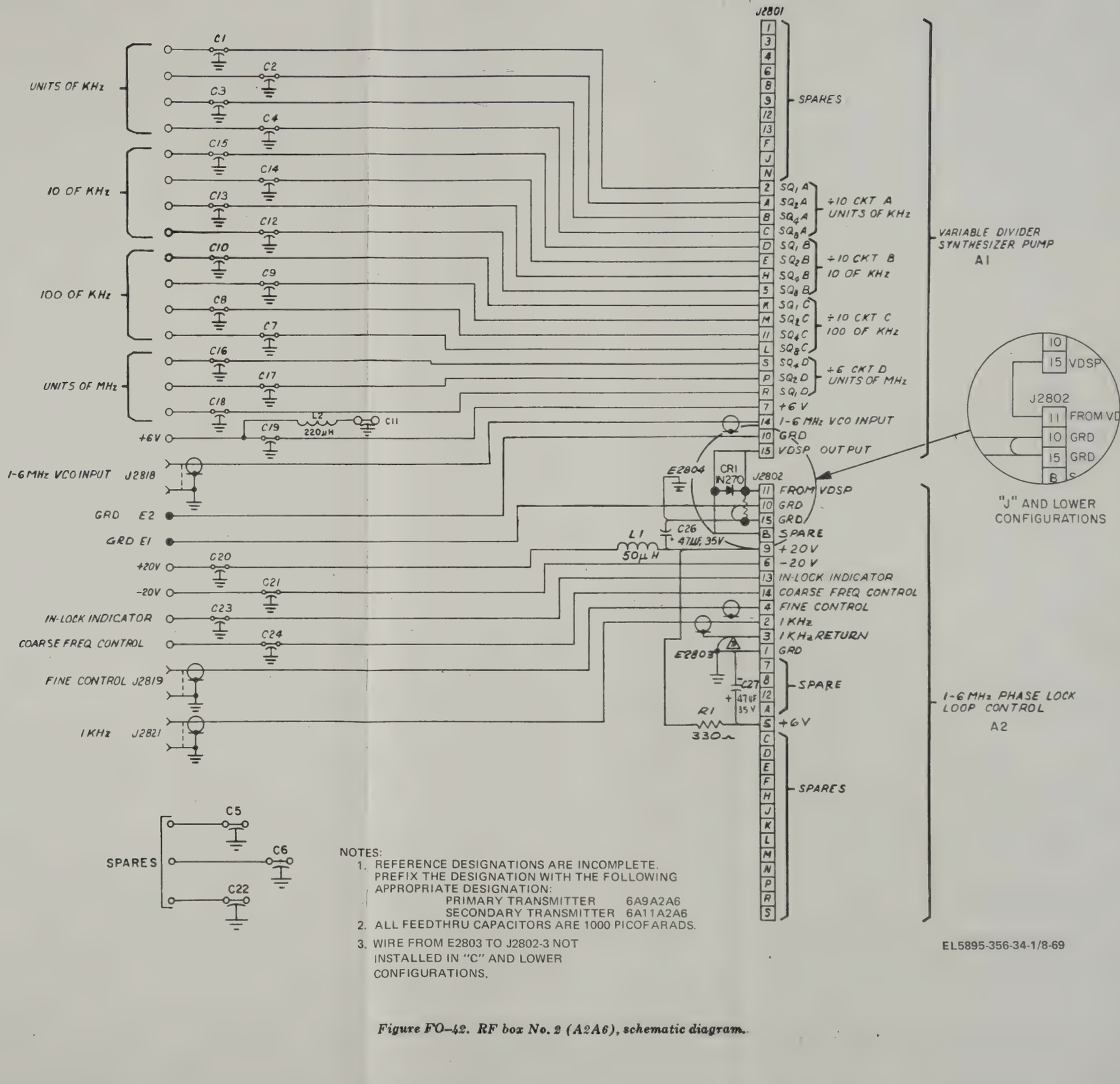
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:

PRIMARY TRANSMITTER	6A9A2A5
SECONDARY TRANSMITTER	6A11A2A5

2. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.
3. C25 AND JUMPER NOT PRESENT IN "V" AND LOWER CONFIGURATIONS.

EL5895-356-34-1/8-68

Figure FO-41. RF box No. 1 (A2A5), schematic diagram.

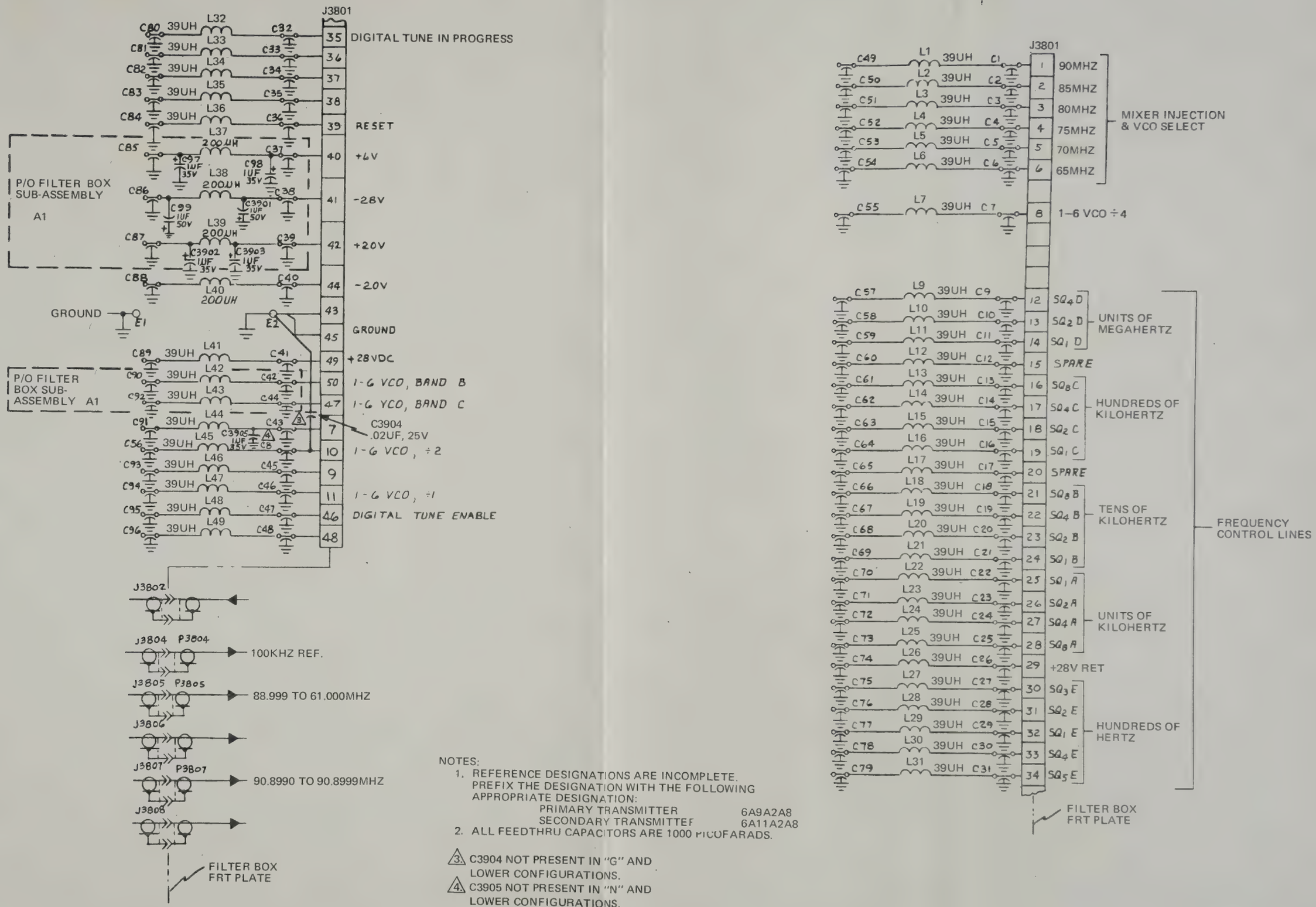


NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A6
   SECONDARY TRANSMITTER 6A11A2A6
2. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.
3. WIRE FROM E2803 TO J2802-3 NOT INSTALLED IN "C" AND LOWER CONFIGURATIONS.

EL5895-356-34-1/8-69

Figure FO–42. RF box No. 2 (A2A6), schematic diagram.

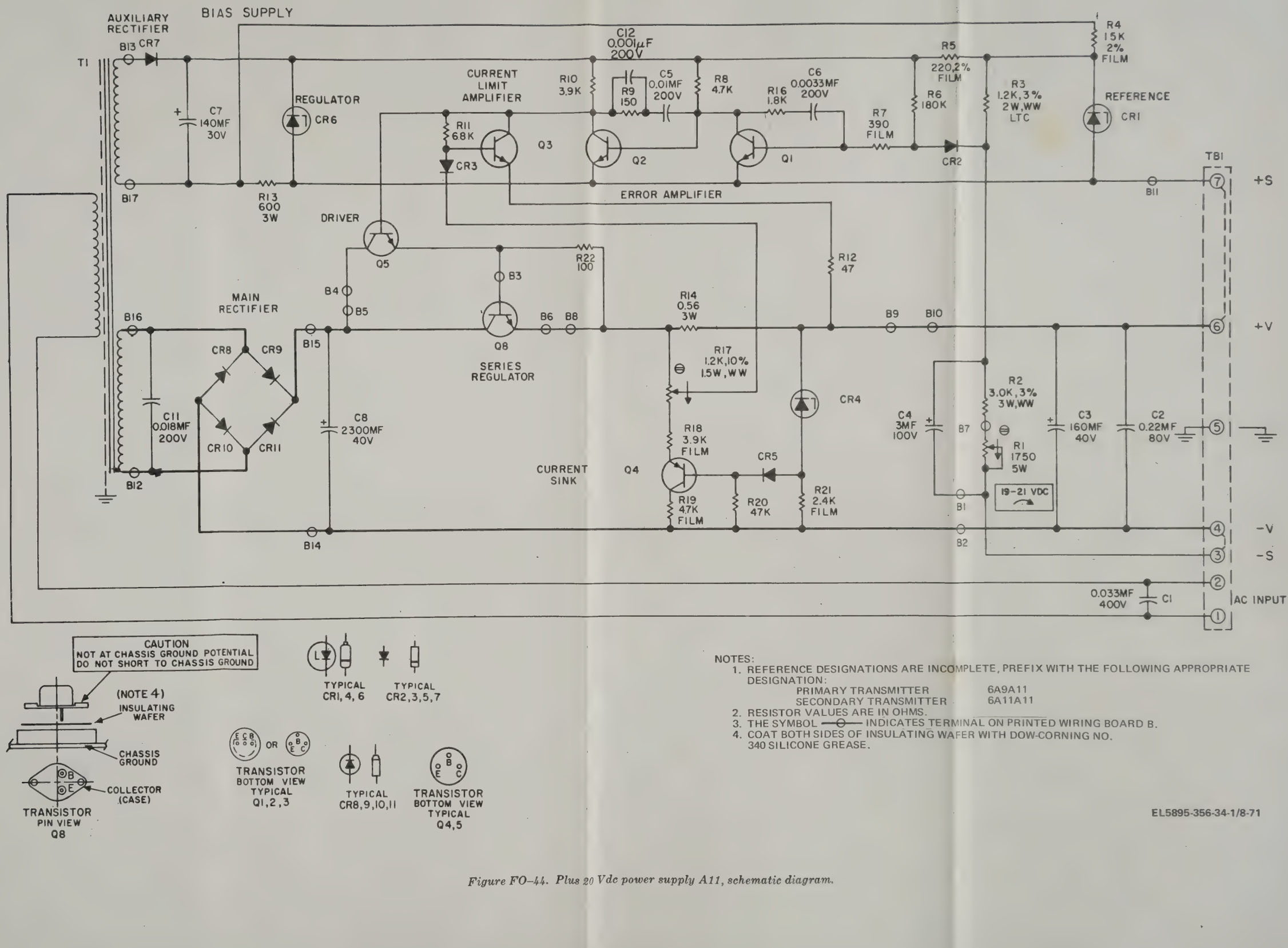


NOTES:
1. REFERENCE DESIGNATIONS ARE INCOMPLETE. PREFIX THE DESIGNATION WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   PRIMARY TRANSMITTER 6A9A2A8
   SECONDARY TRANSMITTEF 6A11A2A8
2. ALL FEEDTHRU CAPACITORS ARE 1000 PICOFARADS.

3. C3904 NOT PRESENT IN "G" AND LOWER CONFIGURATIONS.
4. C3905 NOT PRESENT IN "N" AND LOWER CONFIGURATIONS.

EL5895-356-34-1/8-70

Figure FO–43. Filter box A2A8, schematic diagram.

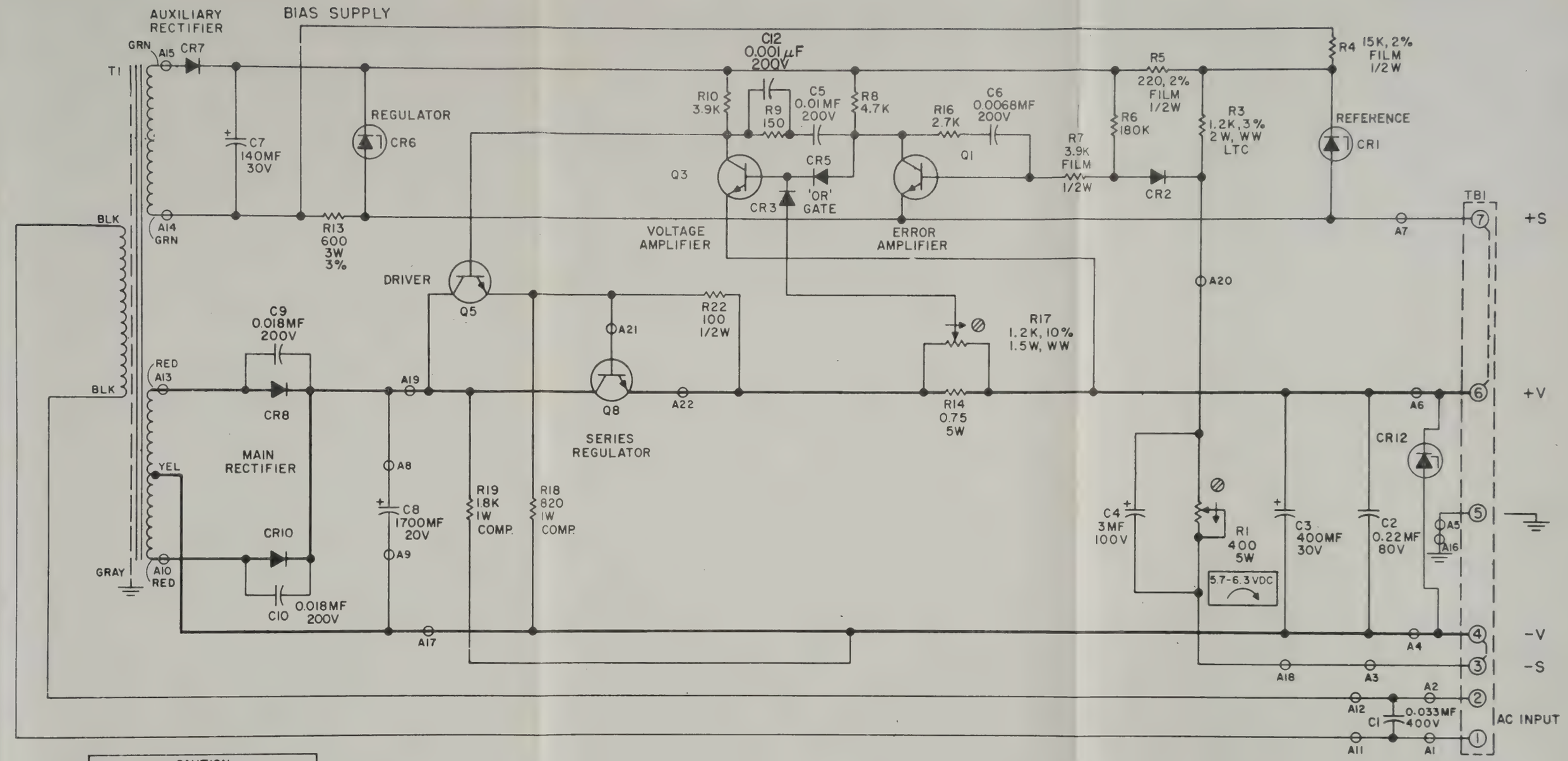


NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE, PREFIX WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   - PRIMARY TRANSMITTER 6A9A11
   - SECONDARY TRANSMITTER 6A11A11
2. RESISTOR VALUES ARE IN OHMS.
3. THE SYMBOL —⊖— INDICATES TERMINAL ON PRINTED WIRING BOARD B.
4. COAT BOTH SIDES OF INSULATING WAFER WITH DOW-CORNING NO. 340 SILICONE GREASE.

EL5895-356-34-1/8-71

Figure FO–44. Plus 20 Vdc power supply A11, schematic diagram.



NOTES:

1. REFERENCE DESIGNATIONS ARE INCOMPLETE, PREFIX WITH THE FOLLOWING APPROPRIATE DESIGNATION:
   - PRIMARY TRANSMITTER 6A9A10
   - SECONDARY TRANSMITTER 6A11A10
2. RESISTOR VALUES ARE IN OHMS.
3. THE SYMBOL —O— INDICATES TERMINAL ON PRINTED WIRING BOARD A.
4. COAT BOTH SIDES OF INSULATING WAFER WITH DOW-CORNING NO. 340 SILICONE GREASE.

EL5895-356-34-1/8-72

Figure FO–45. Plus 6.4 Vdc power supply A10, schematic diagram.

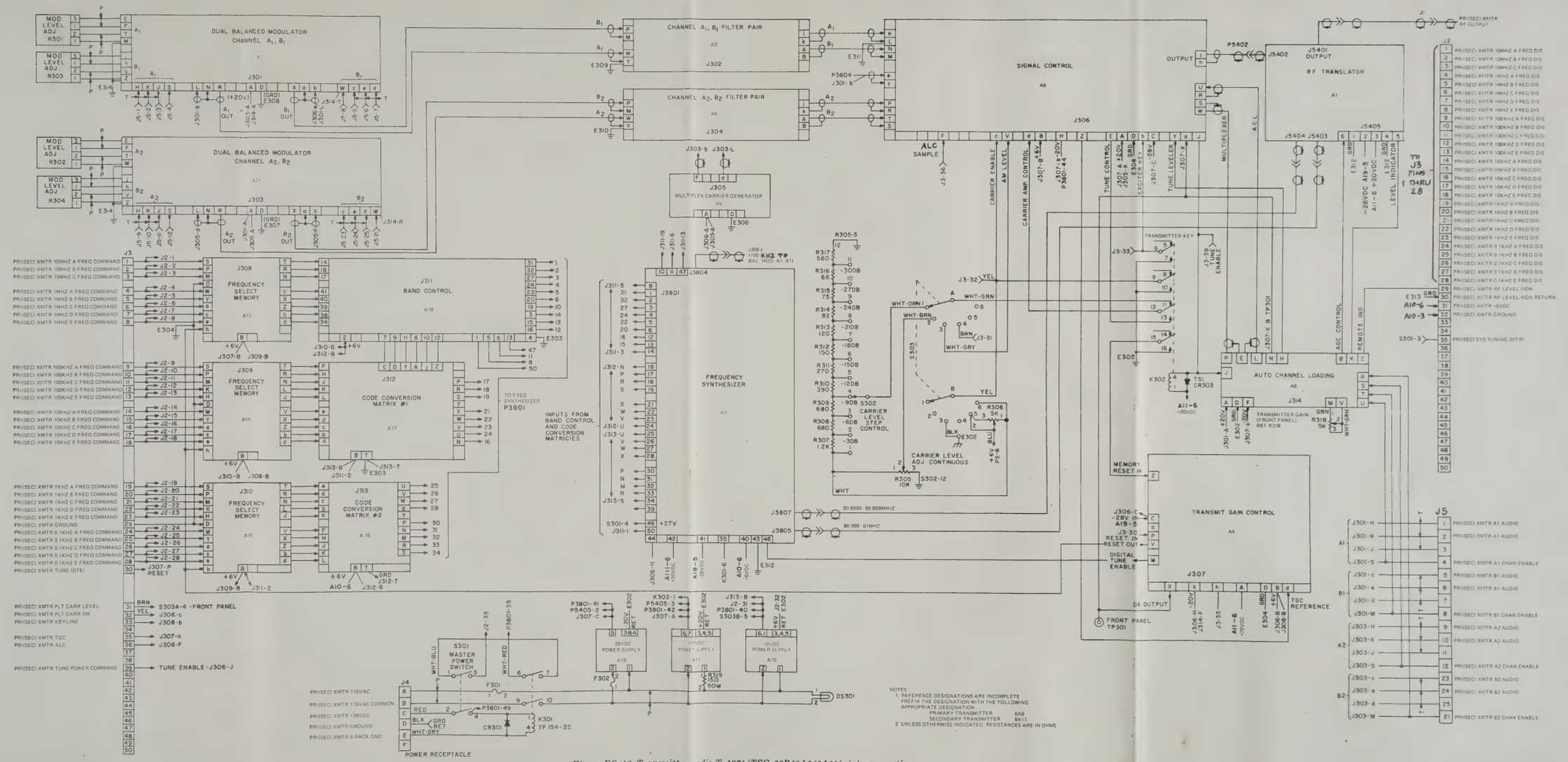
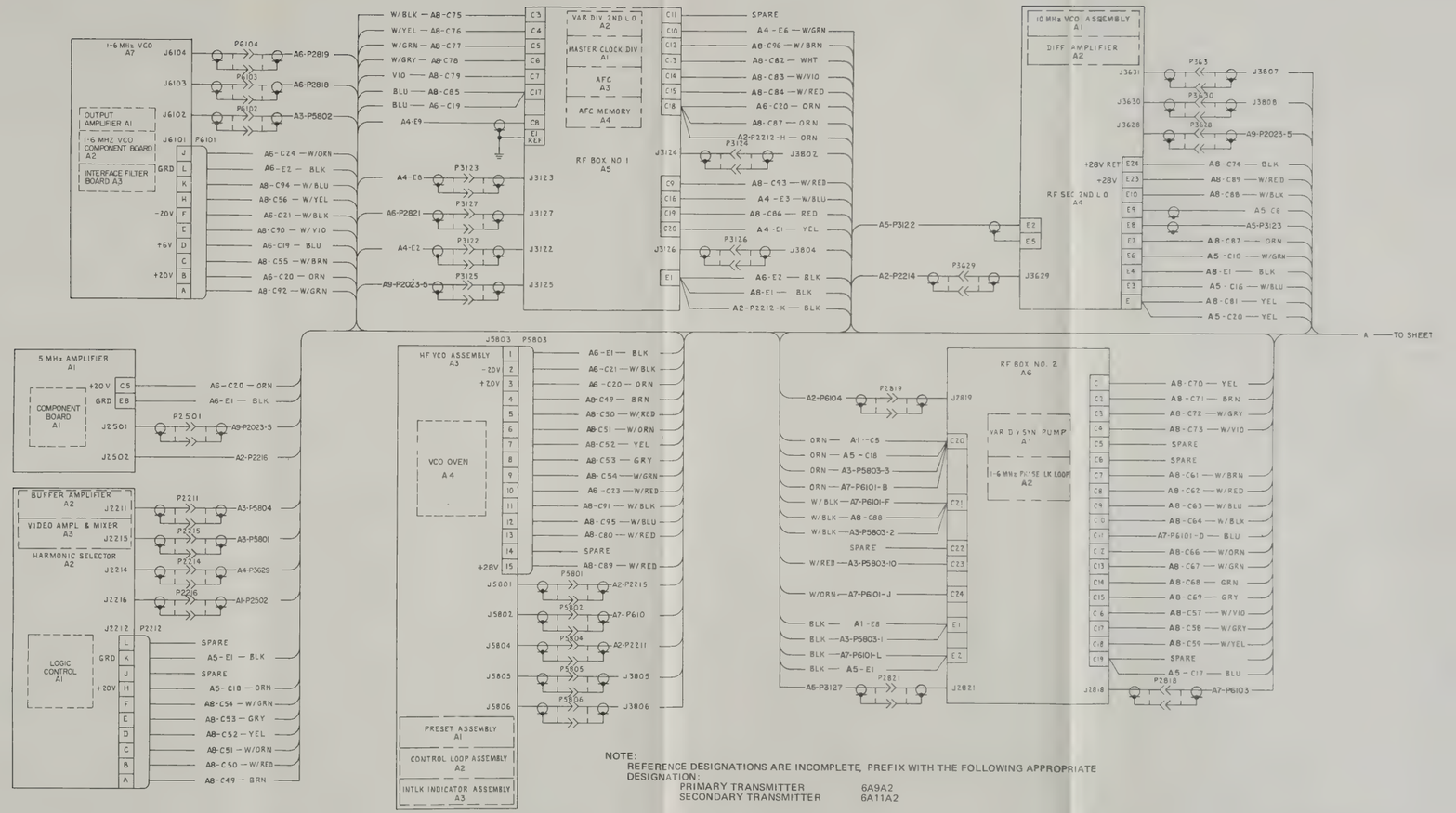


Figure FO–46. Transmitter, radio T–1021/TSC–38B(6A9/6A11), interconnection diagram.

EL5895-356-34-1/8-73



NOTE:
REFERENCE DESIGNATIONS ARE INCOMPLETE, PREFIX WITH THE FOLLOWING APPROPRIATE DESIGNATION:

PRIMARY TRANSMITTER	6A9A2
SECONDARY TRANSMITTER	6A11A2

EL5895-356-34-1/8-74 (1)

Figure FO-47(1). Frequency synthesizer A2, interconnection diagram (sheet 1 of 2).

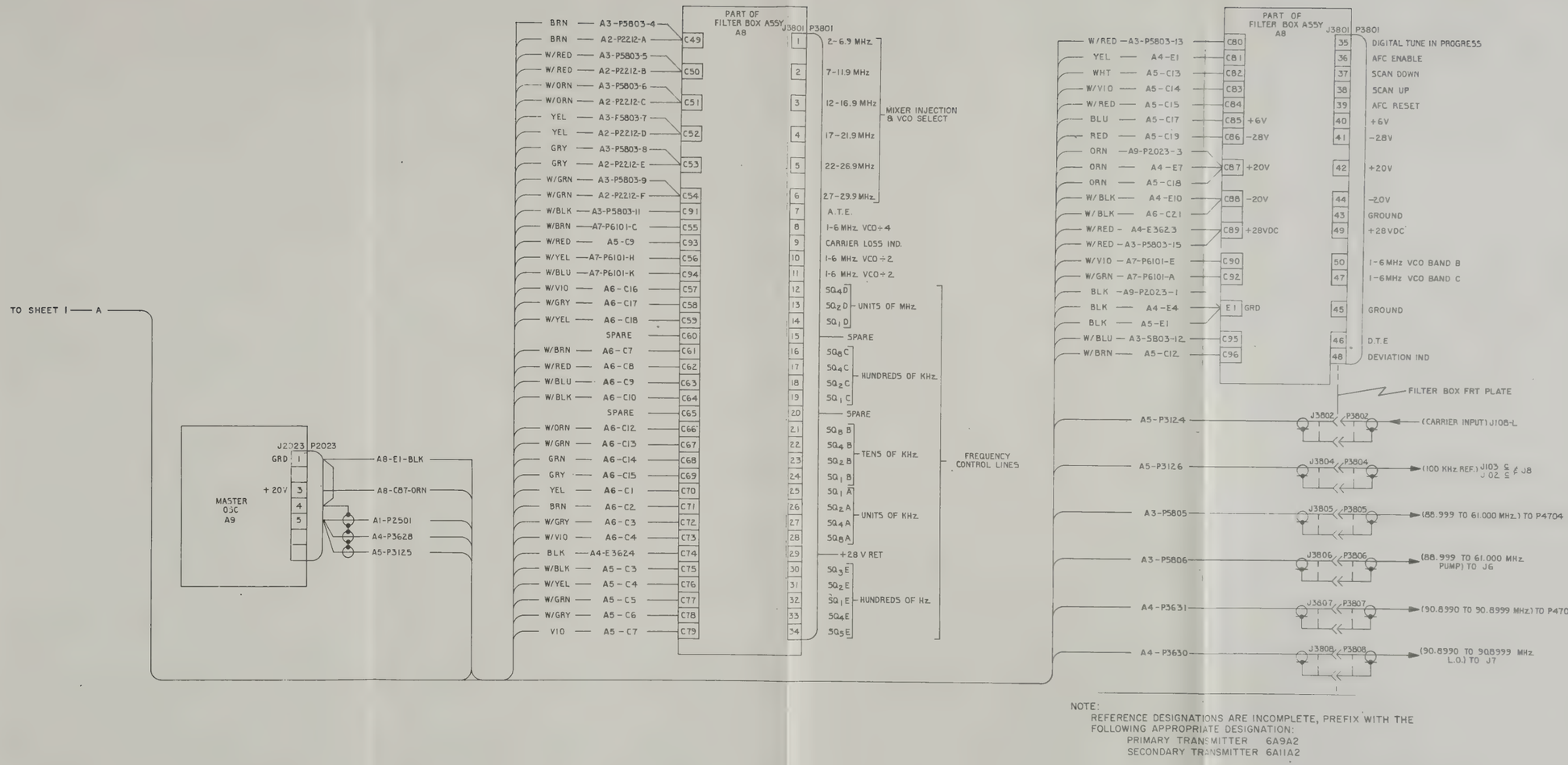


Figure FO–47③. Frequency synthesizer A2, interconnection diagram (sheet 2 of 2).

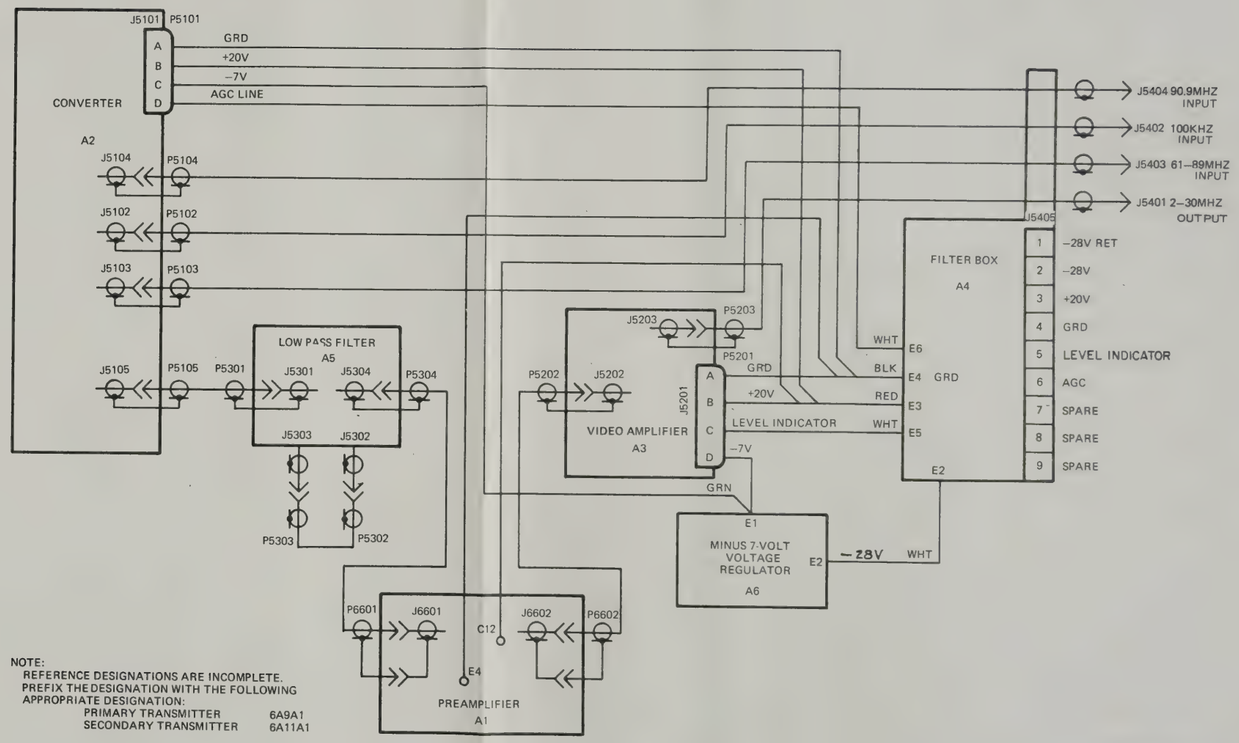
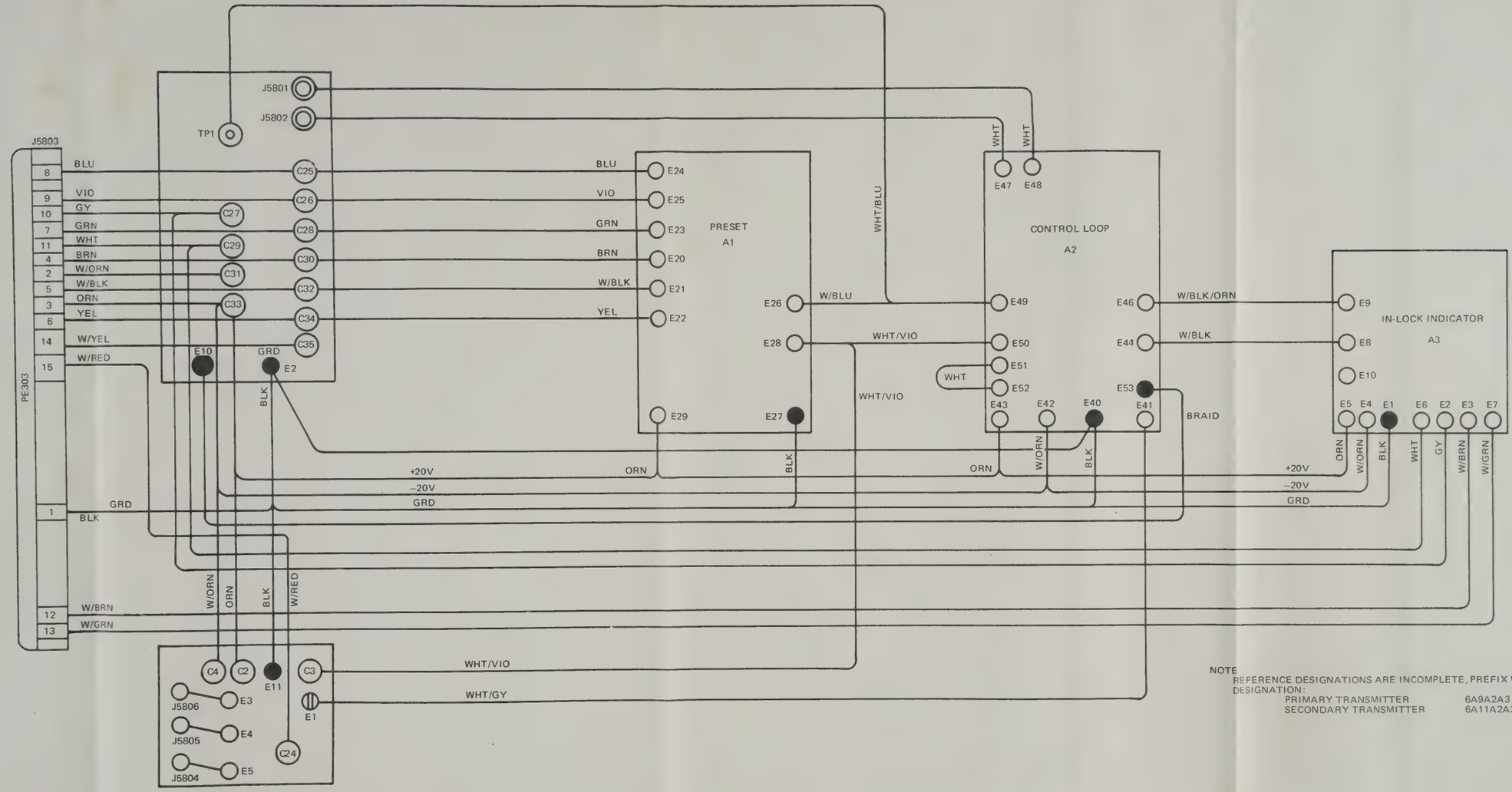


Figure FO–48. Rf translator A1, interconnection diagram.



J5803	
PIN	FUNCTION
1	GRD
2	–20V
3	+20V
4	BAND I ENABLE
5	BAND II ENABLE
6	BAND III ENABLE
7	BAND IV ENABLE
8	BAND V ENABLE
9	BAND VI ENABLE
10	1–6MHZ VCO ERROR SIGNAL
11	A. T. E.
12	D. T. E.
13	D. T. I. P.
14	SPARE
15	+28V

CONN DESTINATION TABLE	
CONN	TO (EXTERNAL)
J5801	DIFF VIDEO INPUT
J5802	1–6MHZ REF INPUT
J5804	HARMONIC GEN
J5805	PUMP AMPL
J5806	PUMP AMPL

NOTE
REFERENCE DESIGNATIONS ARE INCOMPLETE, PREFIX WITH THE FOLLOWING APPROPRIATE DESIGNATION:

PRIMARY TRANSMITTER	6A9A2A3
SECONDARY TRANSMITTER	6A11A2A3

EL5895-356-34-1/8-76

Figure FO–49. Hf VCO A2A3, interconnection diagram.

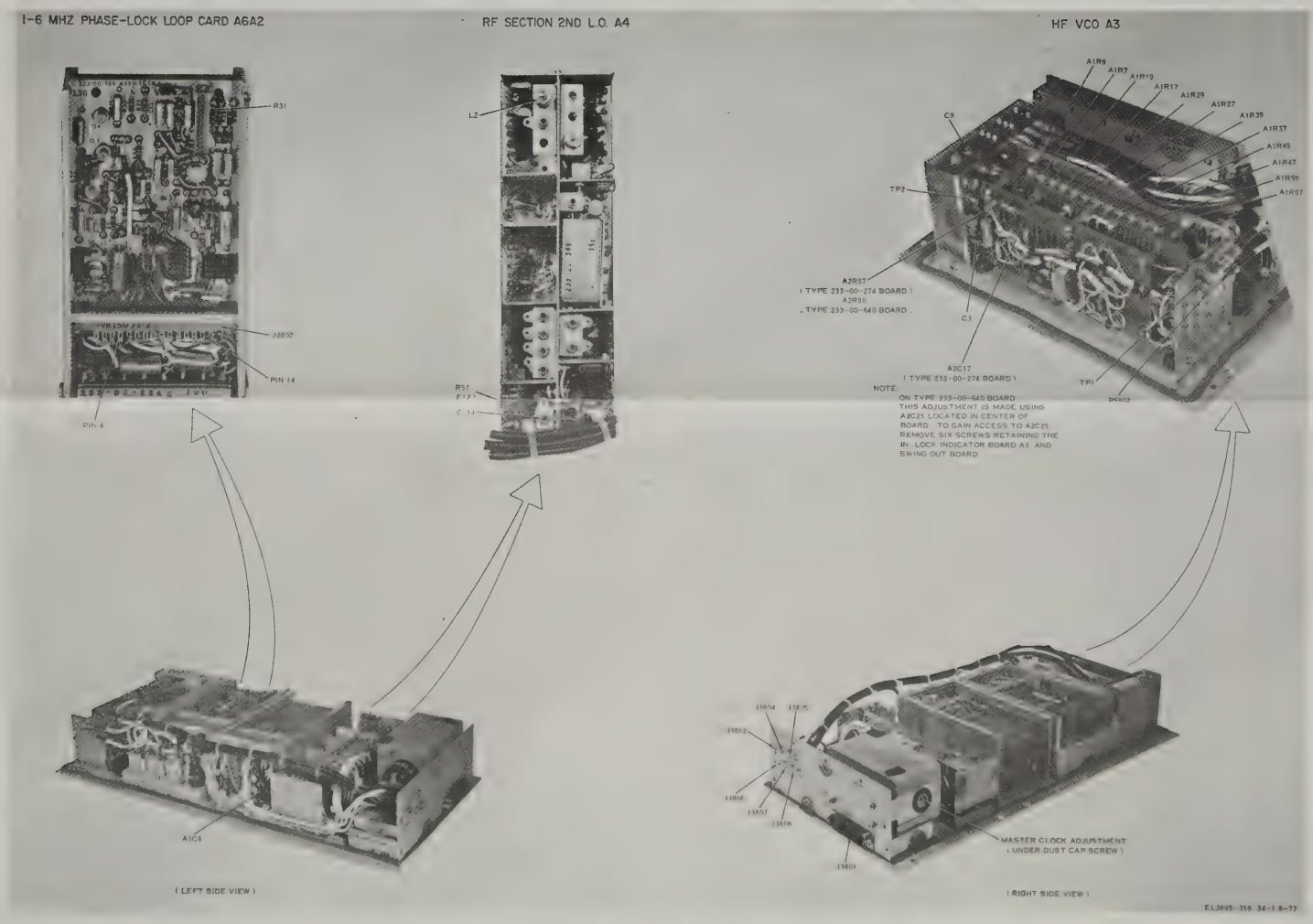


Figure FO–50. Frequency synthesizer A2, location of test points and adjustments.

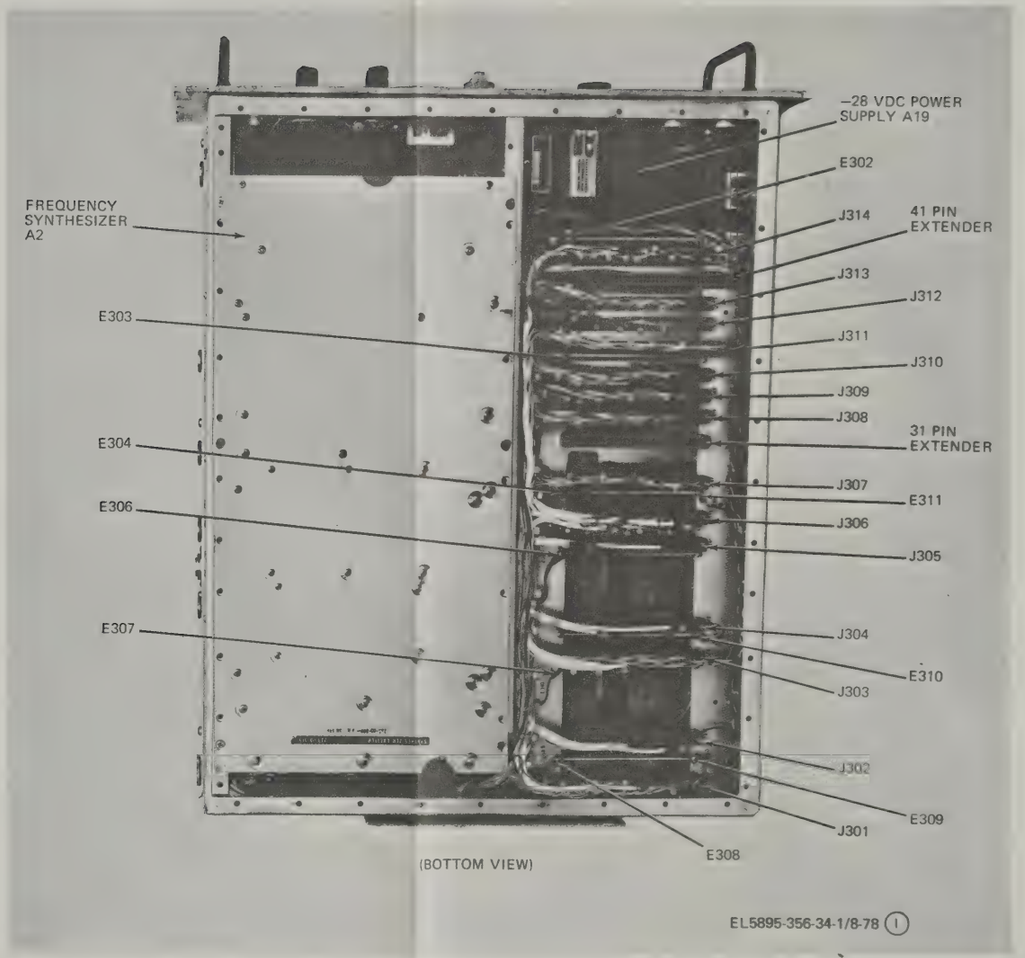


Figure FO–51①. Transmitter chassis assembly (6A9/6A11) parts location diagram (sheet 1 of 3).

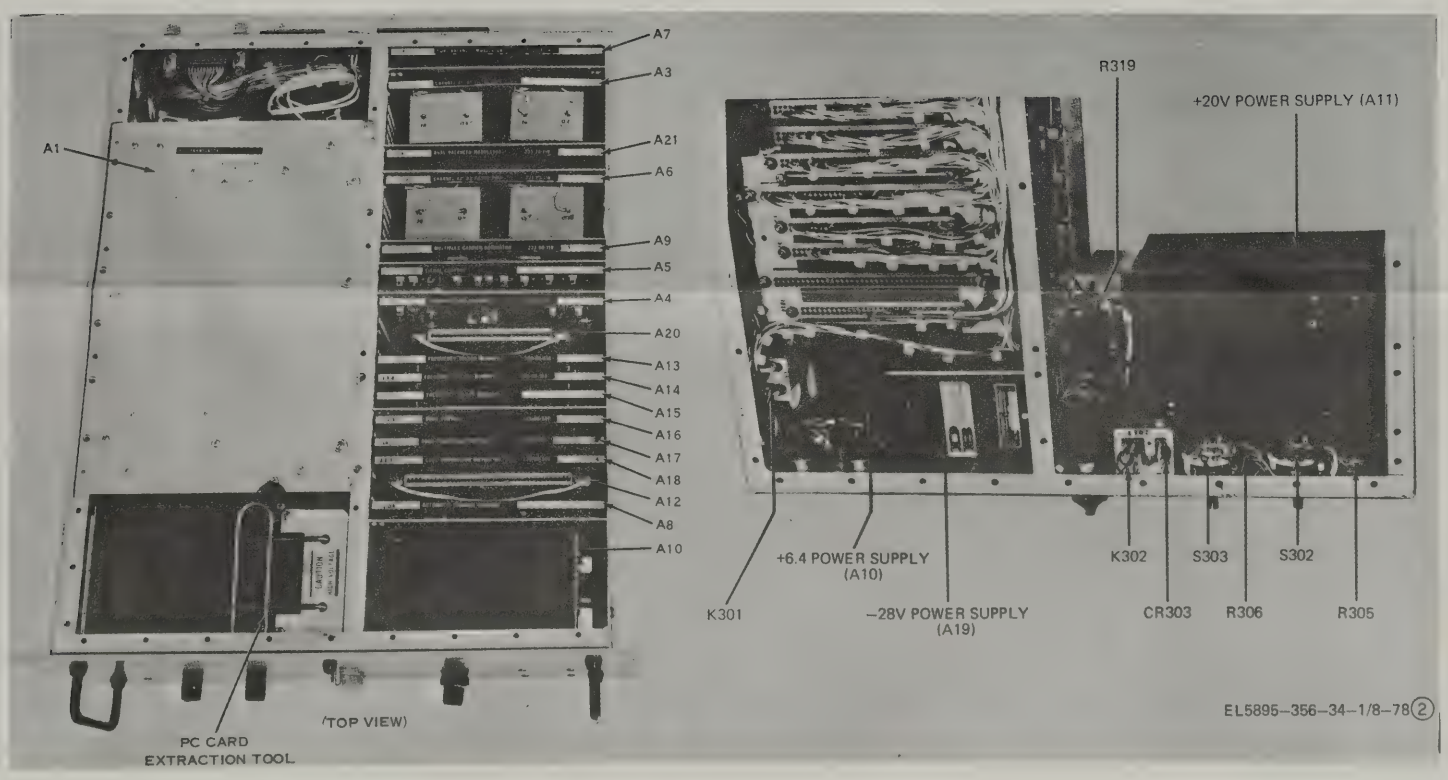


Figure FO–51②. Transmitter chassis assembly (6A9/6A11) parts location diagram (sheet 2 of 3).

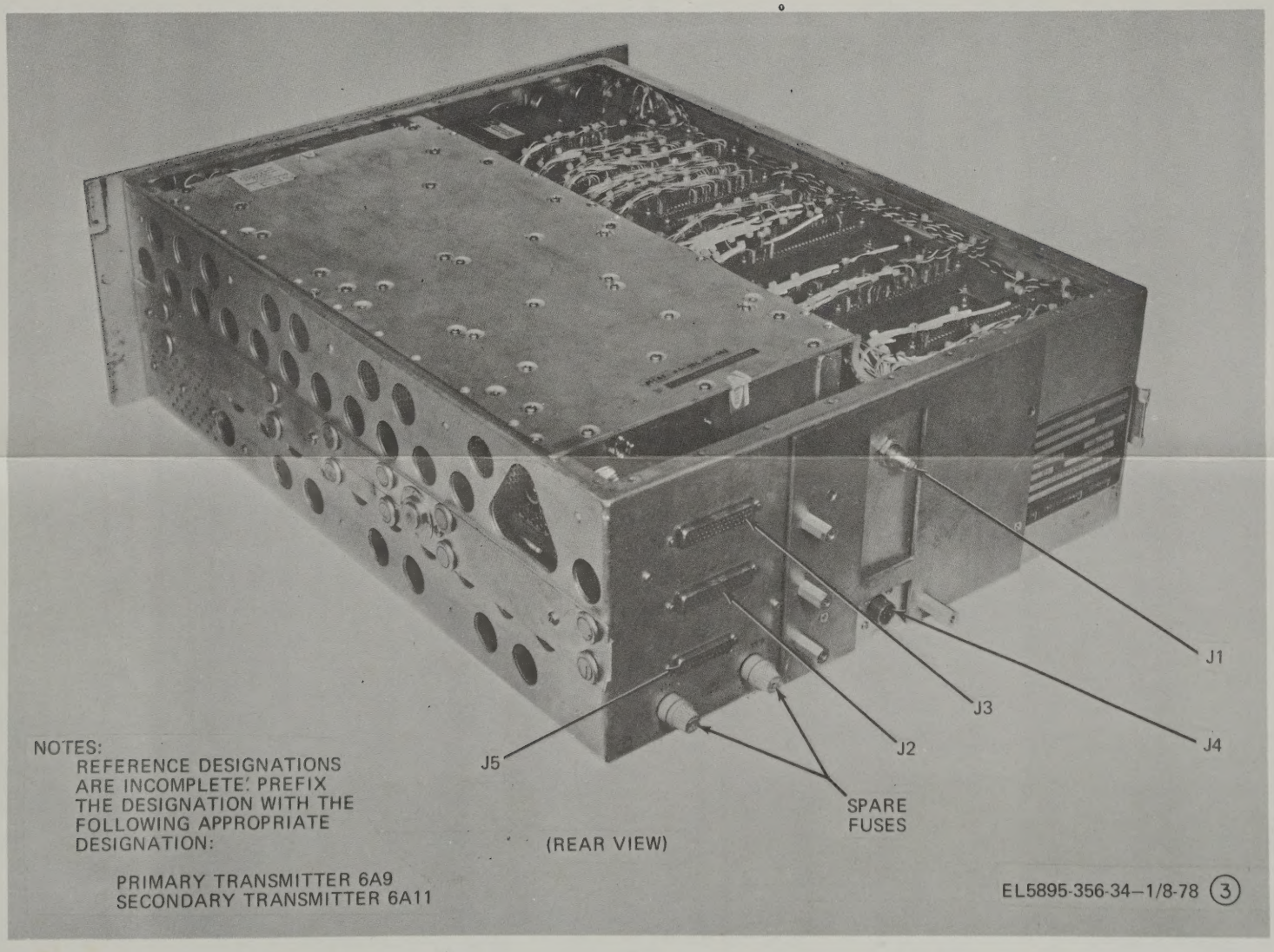


Figure FO–51③. Transmitter chassis assembly (6A9/6A11) parts location diagram (sheet 3 of 3).